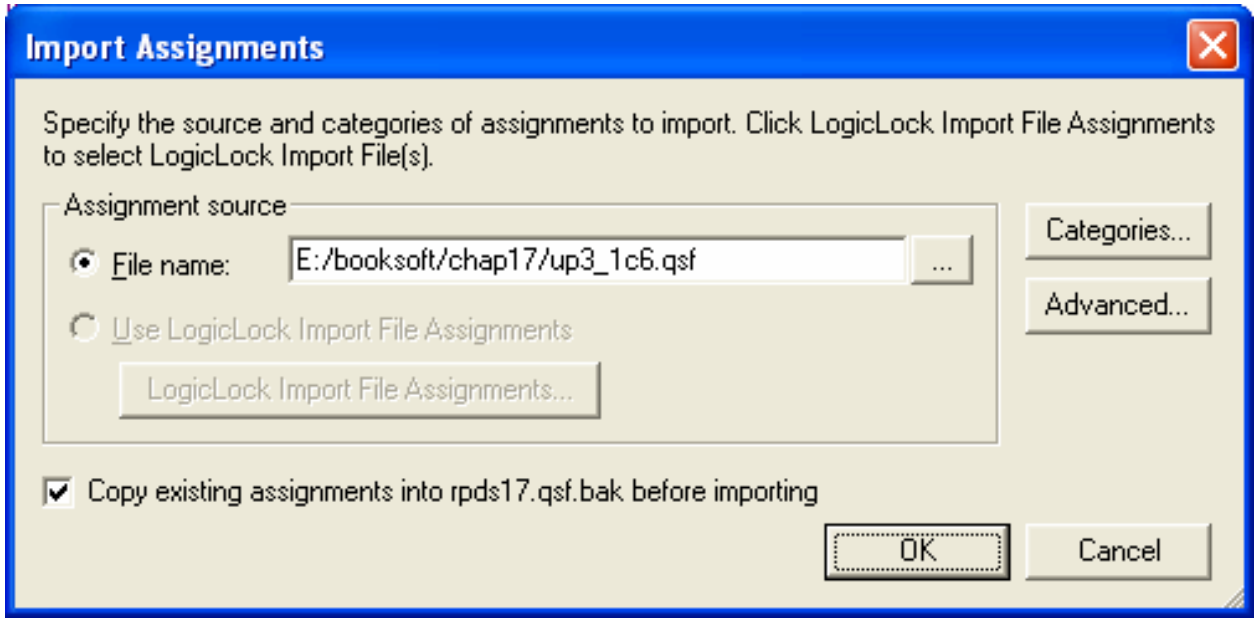


Figure 17.1 Import the default pin and project assignments for the UP 3 board.

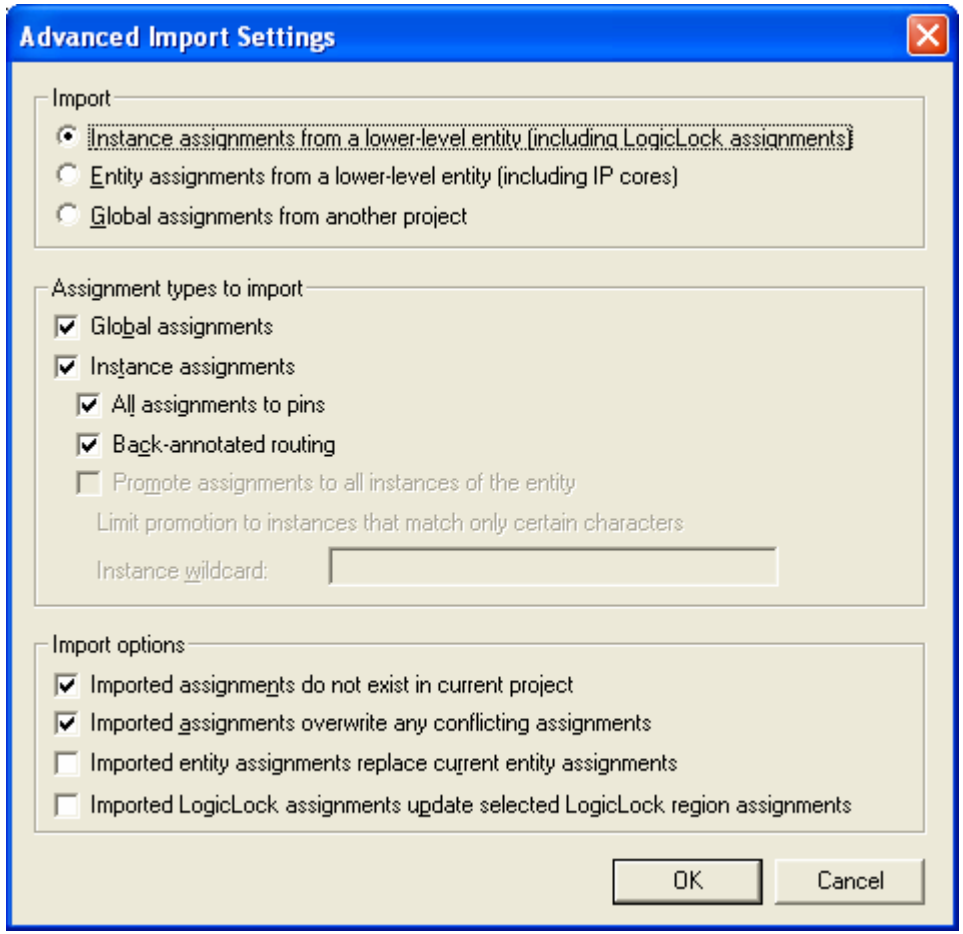


Figure 17.2 It is important that the Advanced Import Options be set as shown here.

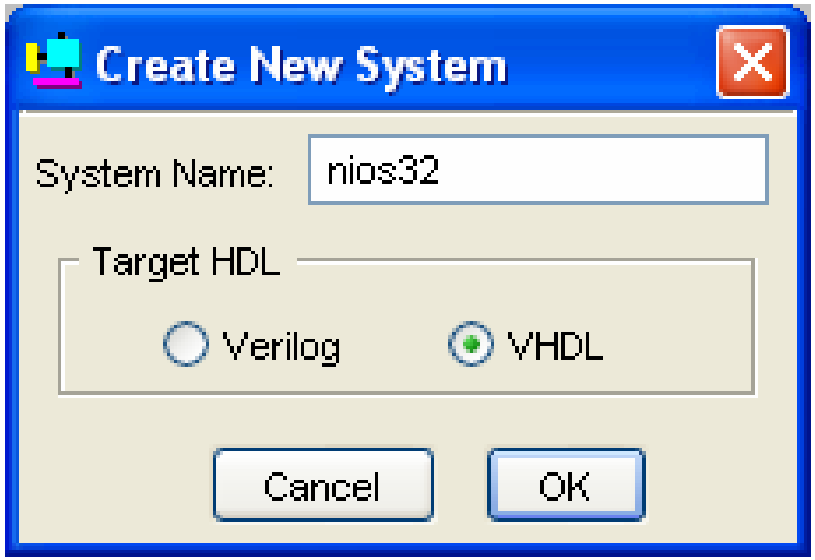


Figure 17.3 Specifying the name of the Nios II processor for your system

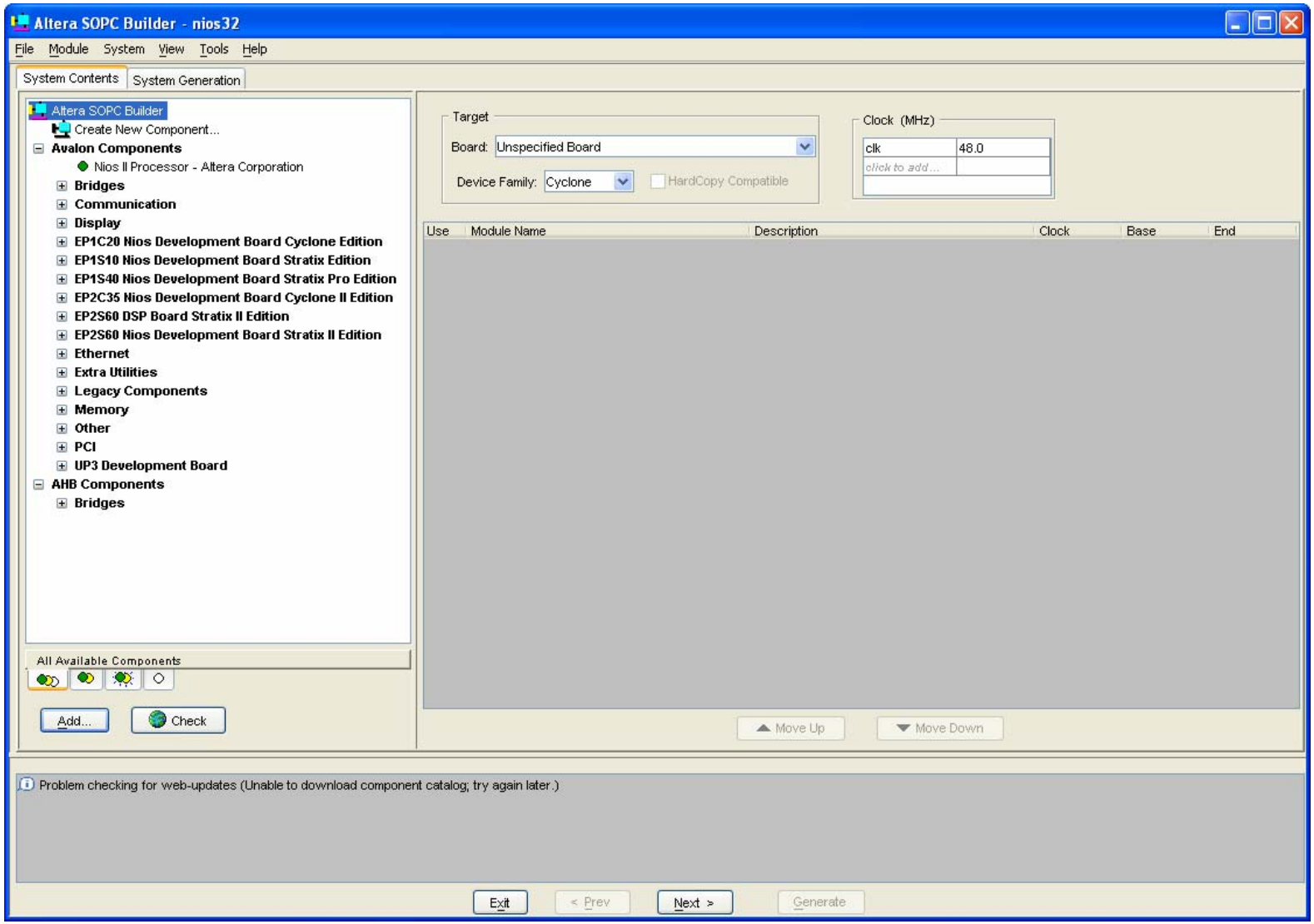


Figure 17.4 Beginning a Nios II design in the SOPC Builder.

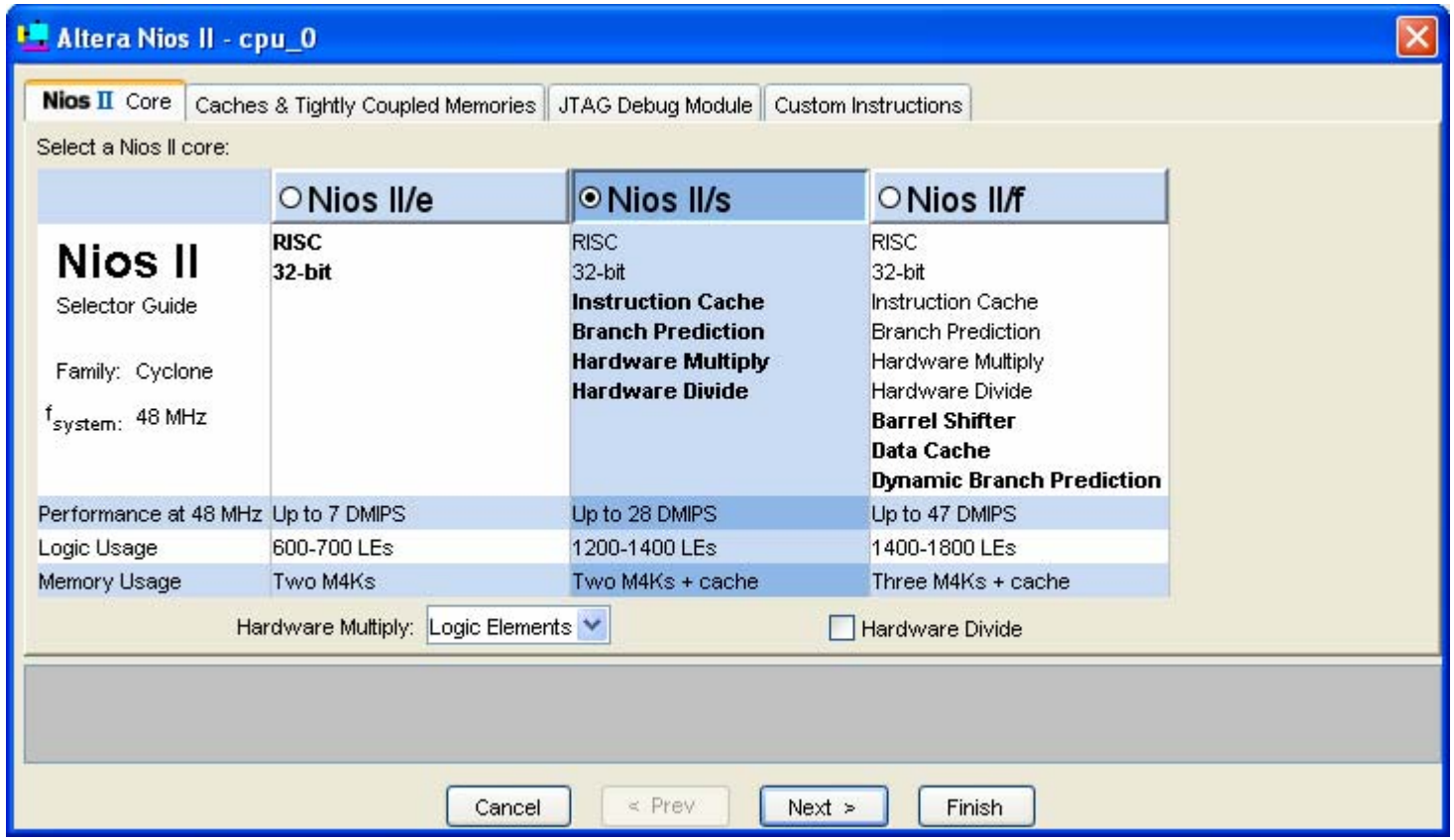


Figure 17.5 Nios II supports three different general configurations. Select Nios II/s for this tutorial

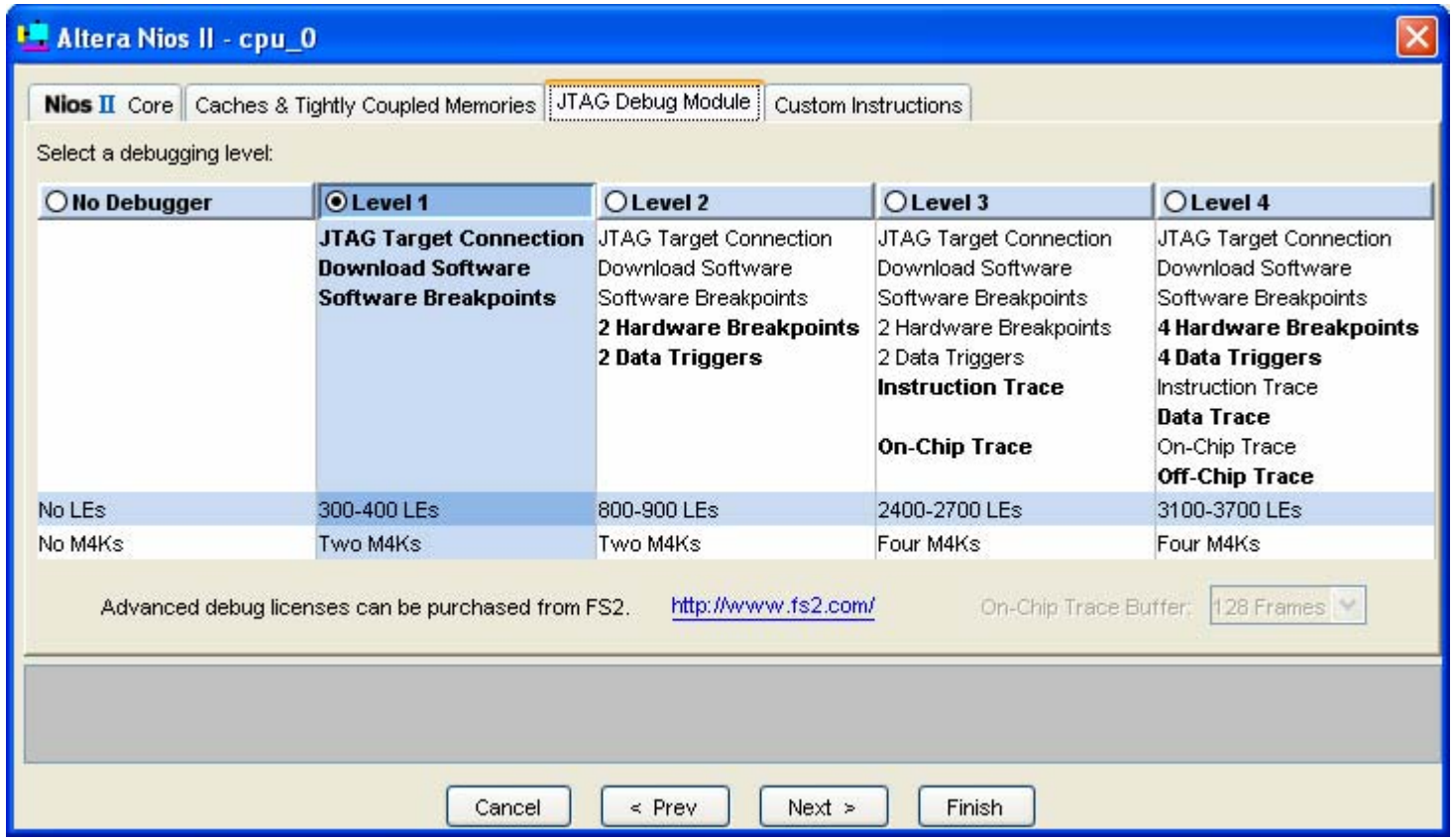


Figure 17.6 Nios II supports four levels of debugging capabilities. Select Level 1 for this tutorial.

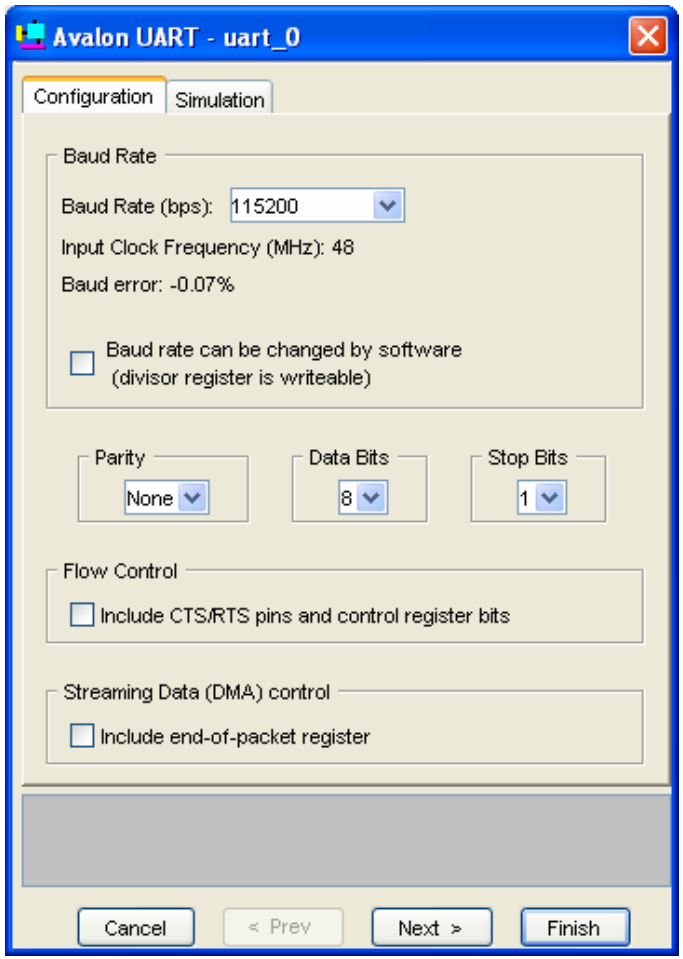


Figure 17.7 **These are the settings for the RS-232 UART device to be added to the Nios II system**

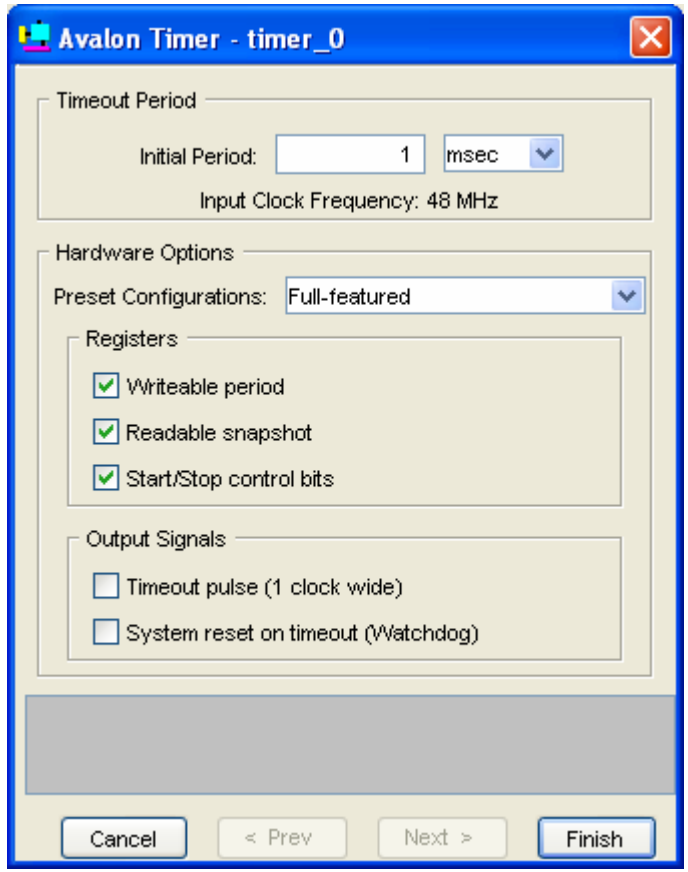


Figure 17.8 These are the settings for the interval timer device to be added to the Nios II system.

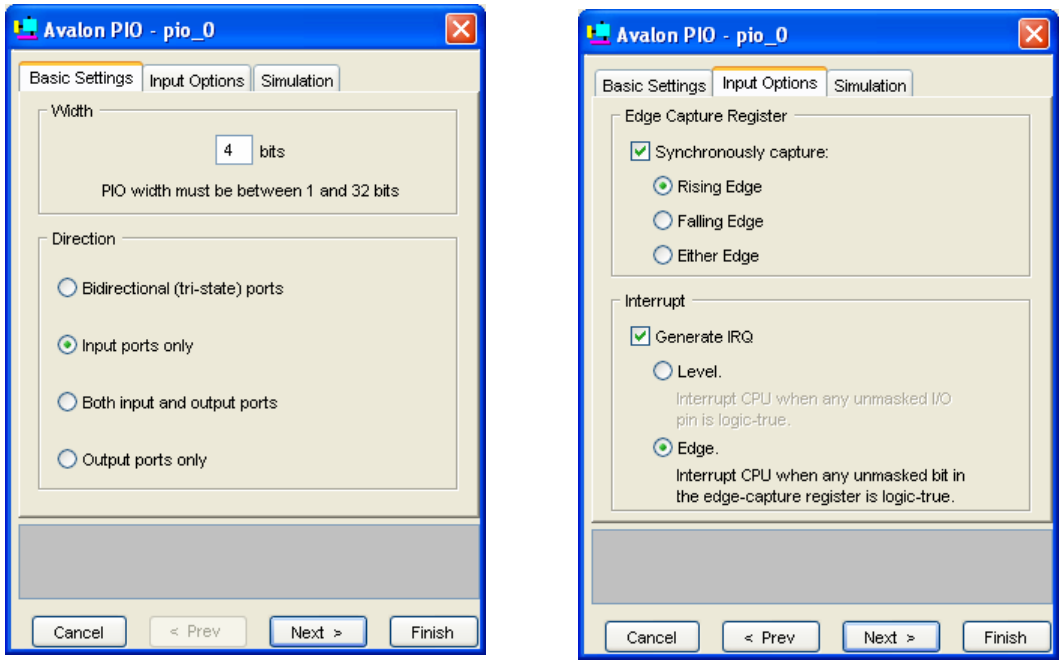
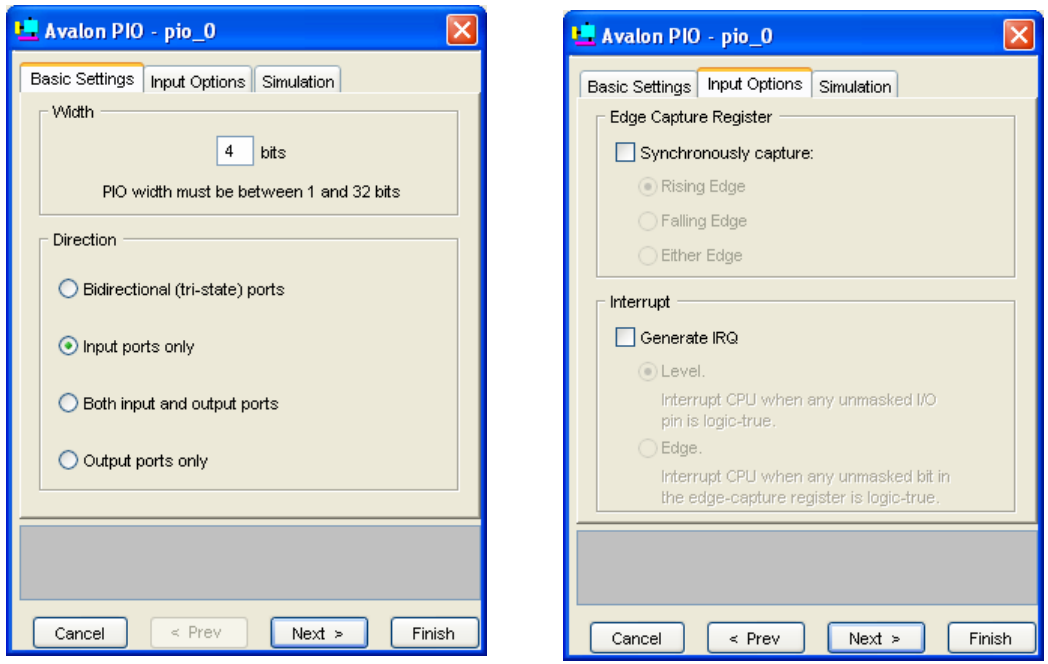
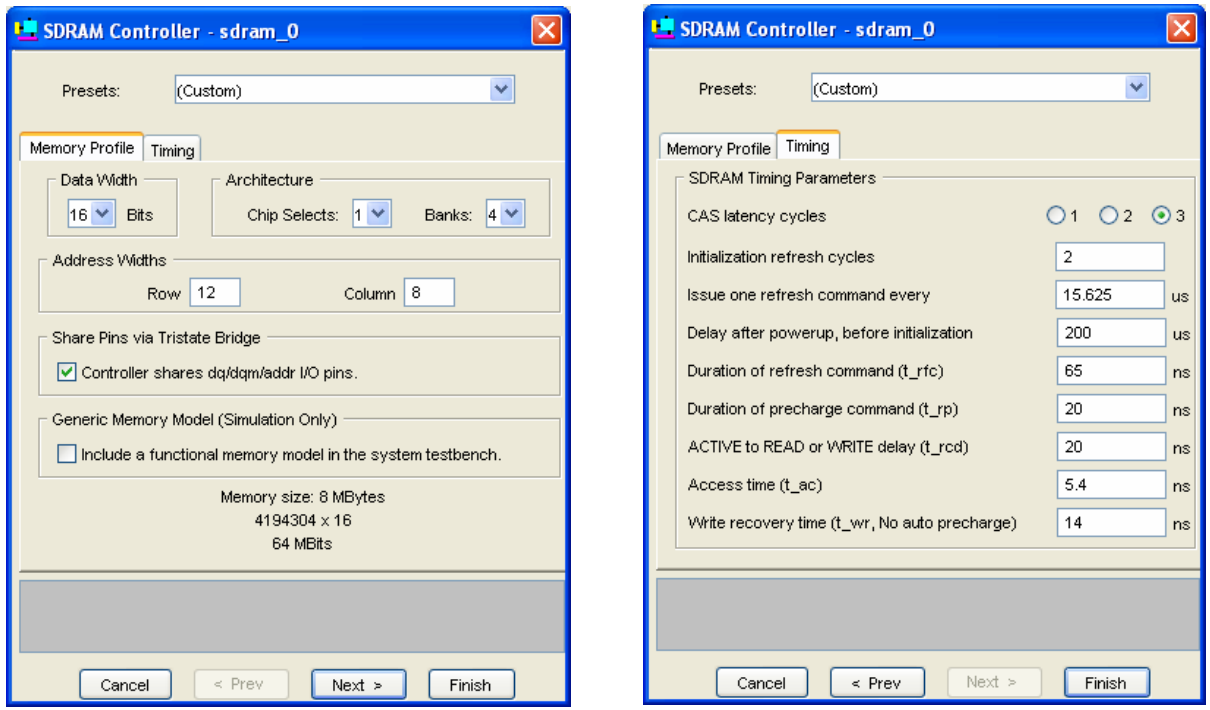


Figure 17.9 These are the settings for the pushbutton PIO device to be added to the Nios II system.



(a) (b)

Figure 17.10 These are the settings for the dipswitch PIO device to be added to the Nios II system.



(a) (b)

Figure 17.11 These are the SDRAM controller settings for use with the SDRAM on the UP 3 board.

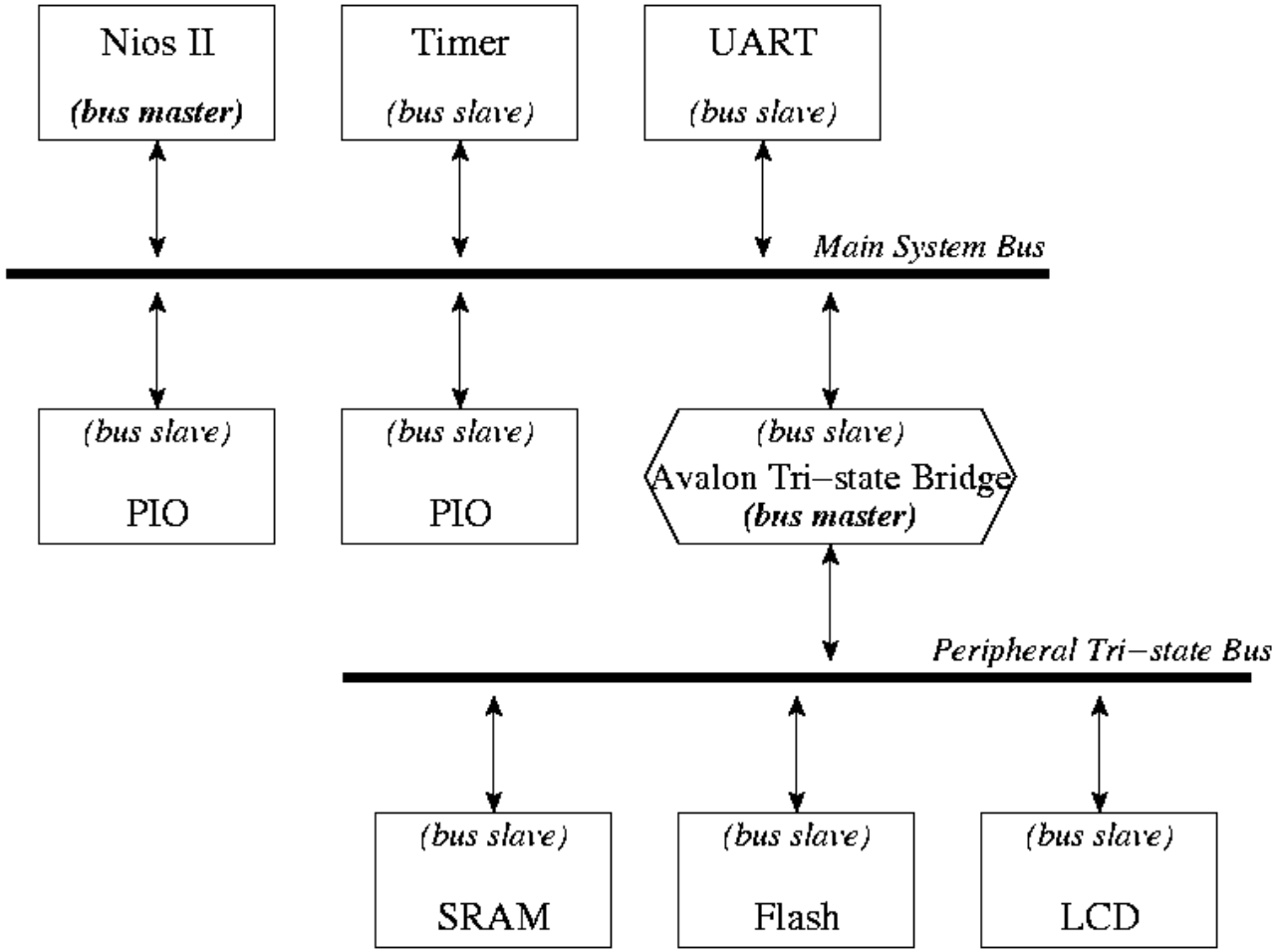
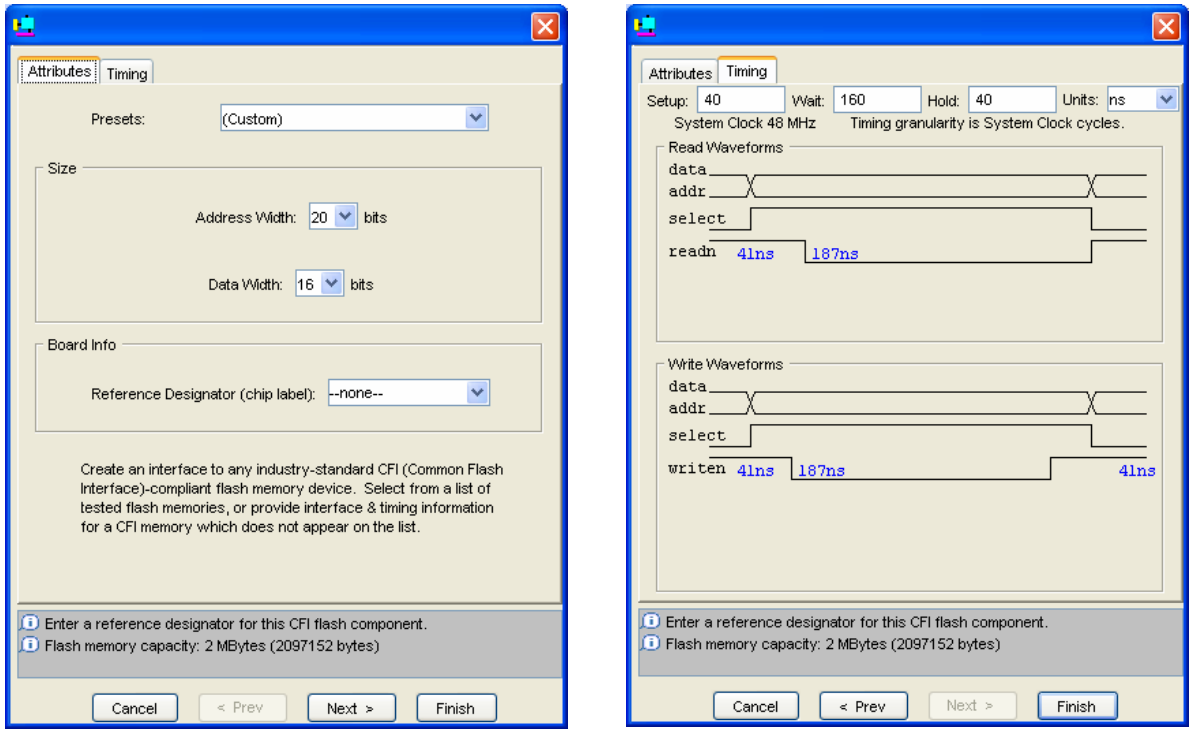


Figure 17.12 This is a conceptual drawing of the bus configuration with the Tristate Bridge connecting the main system bus and the shared peripheral bus.



(a) (b)

Figure 17.13 These are the Flash memory settings for use with the Flash on the UP 3 board.

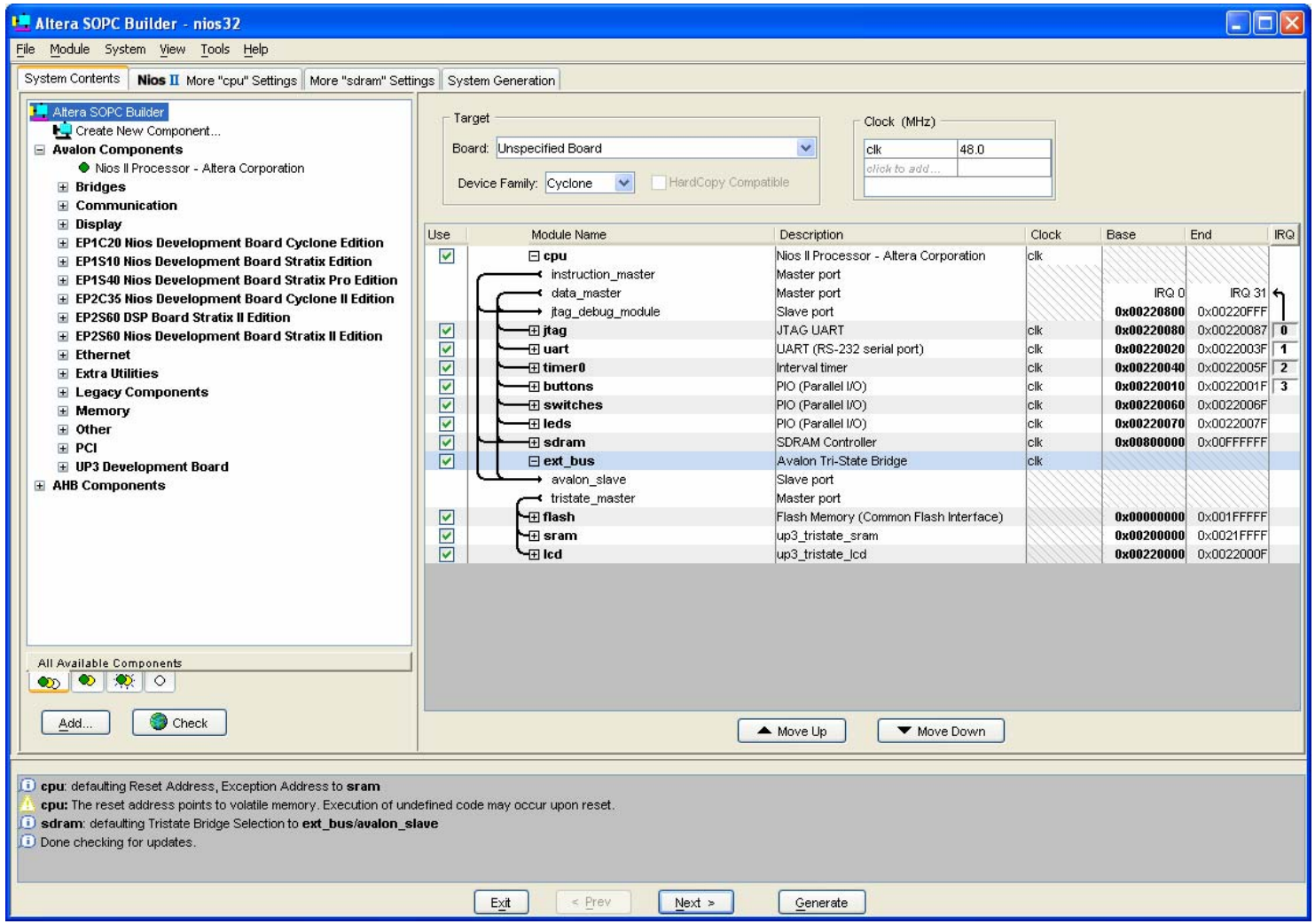


Figure 17.14 This is the completed Nios II design in SOPC Builder.

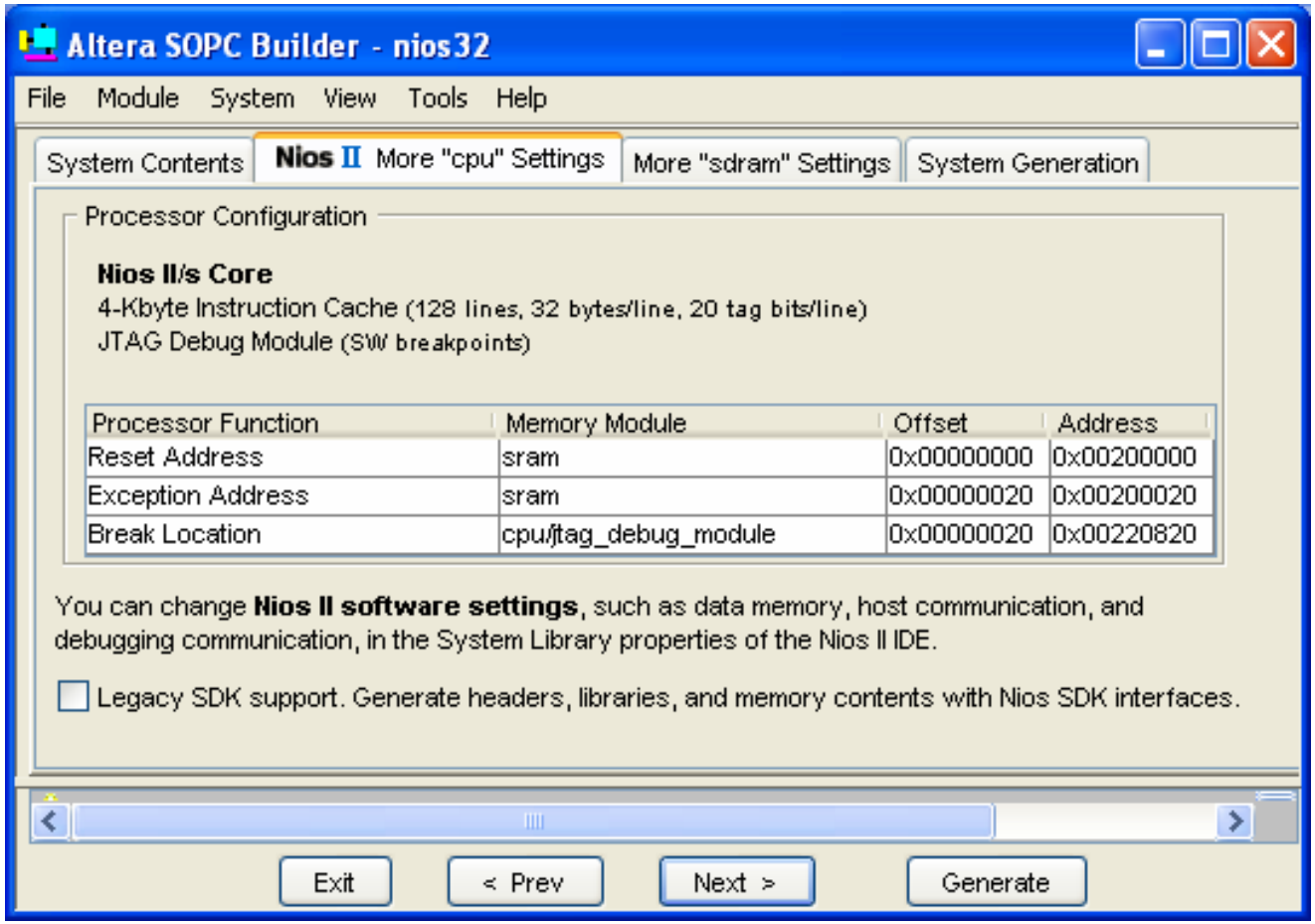


Figure 17.15 These are the processor configuration settings for the Nios II processor.

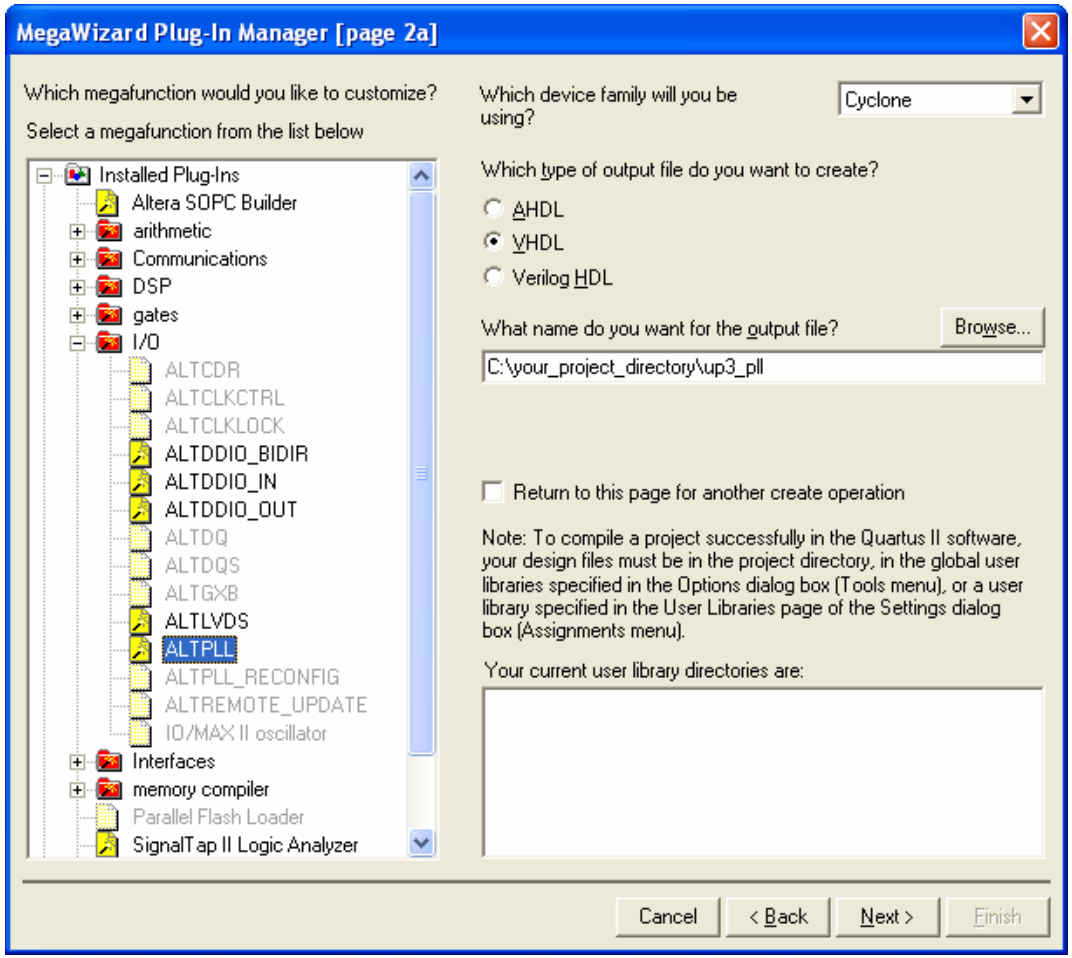


Figure 17.16 These are the initial settings for the ALTPLL module.

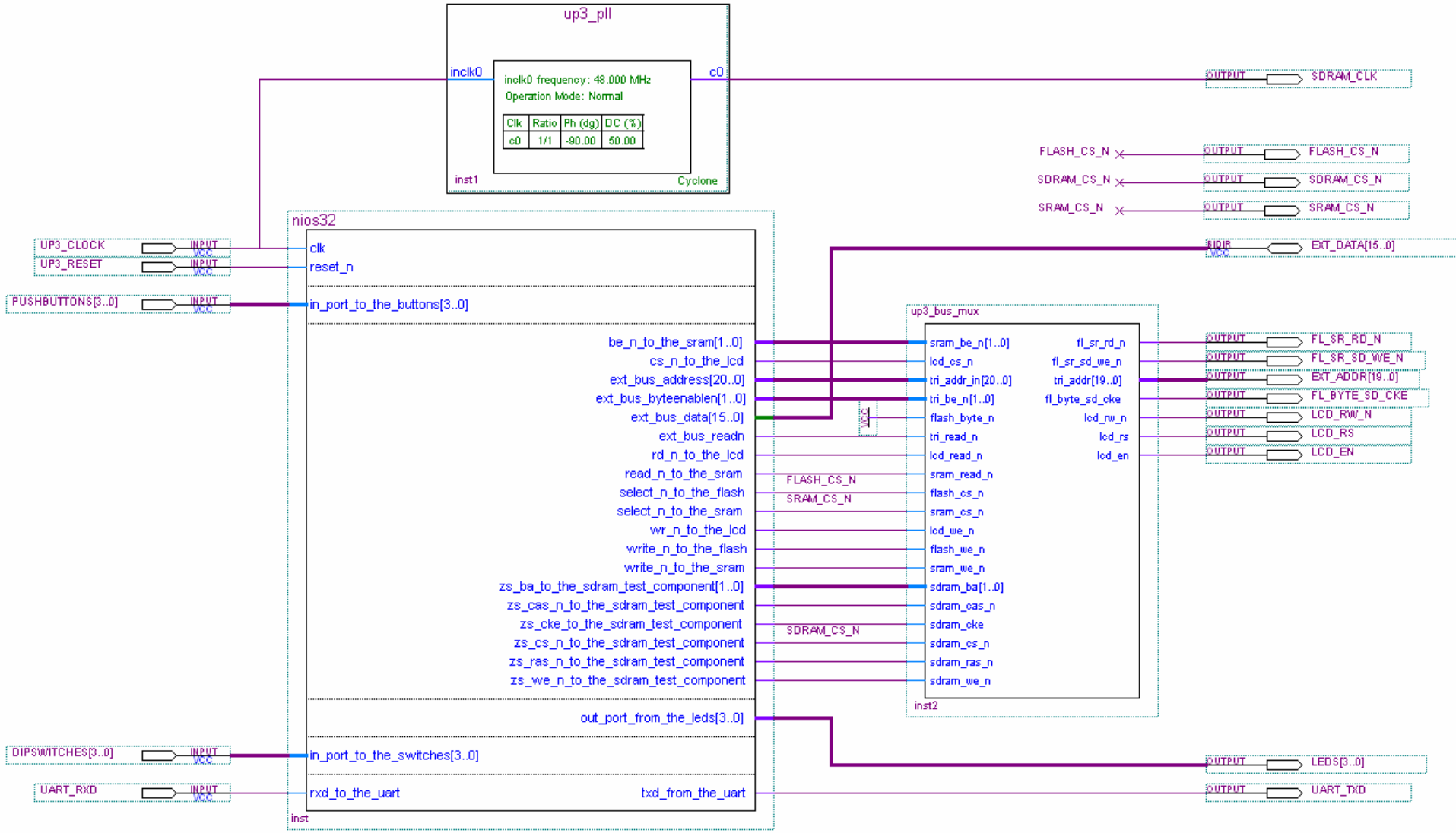


Figure 17.17 The final top-level schematic for the Nios II system.