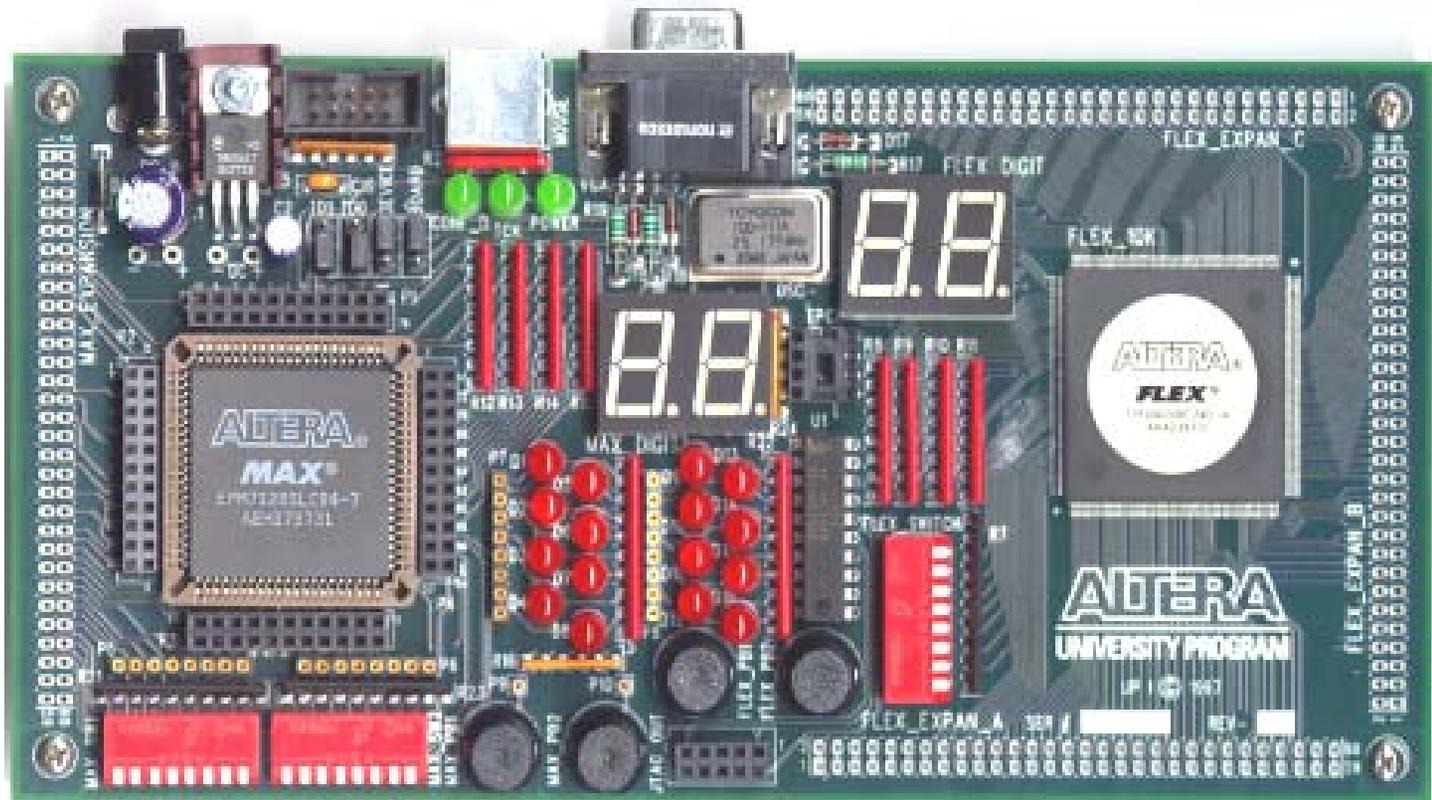


**Figure 1.1** The Altera UP 3 FPGA Development board



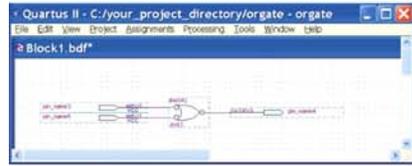
**Figure 1.2** The Altera UP 2 FPGA development board.

## Design

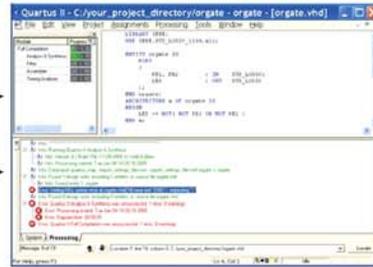
## Compilation

## Simulation

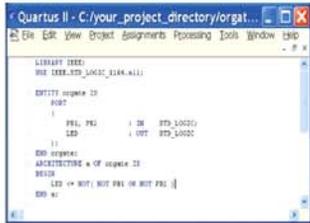
## Verification



Graphical Entry



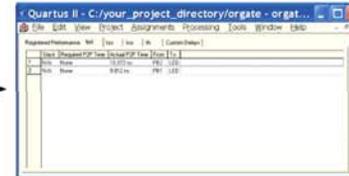
Compiler



HDL Model



Timing Diagram



Timing Analysis

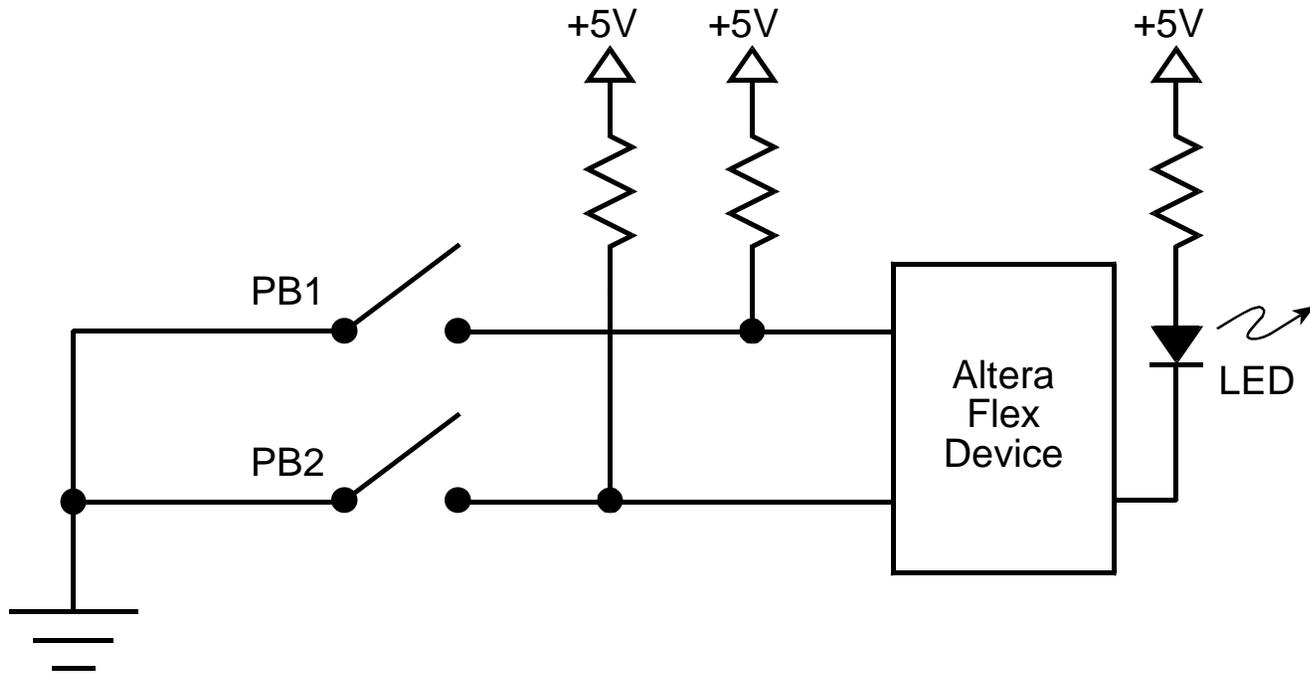


Program FPGA

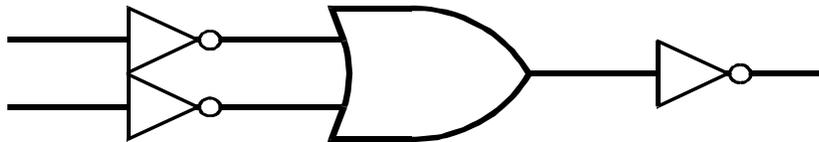


UP 3 Development Board

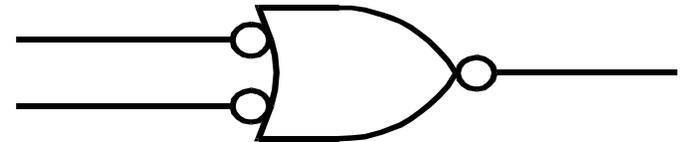
**Figure 1.3** Design process for schematic or HDL entry.



**Figure 1.4** Connections between the pushbuttons, the LEDs, and the Altera FPGA.

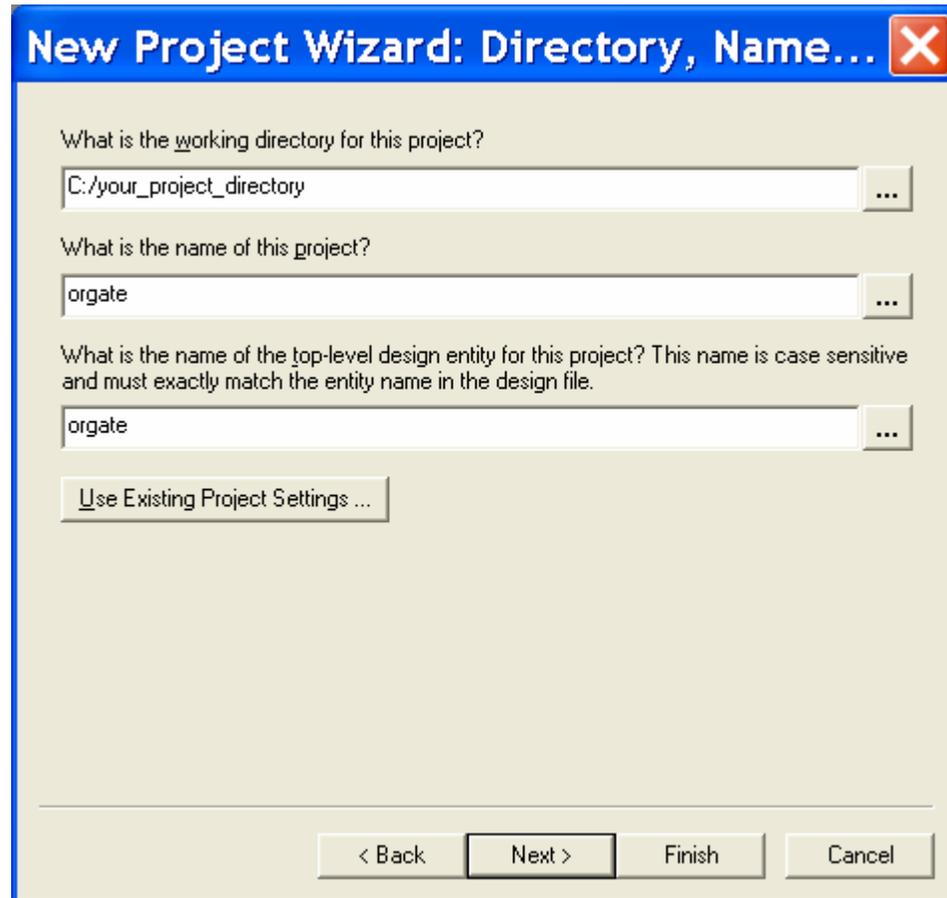


(a)

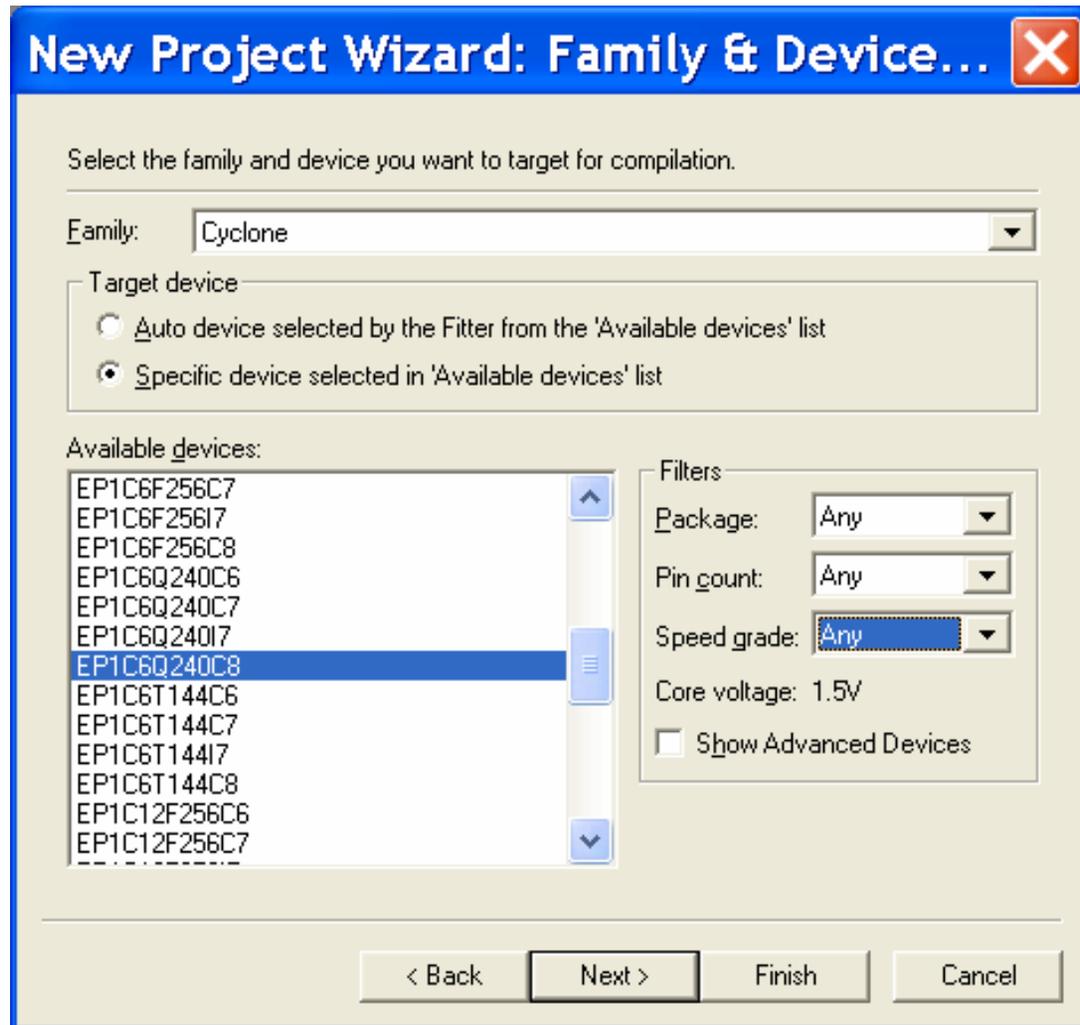


(b)

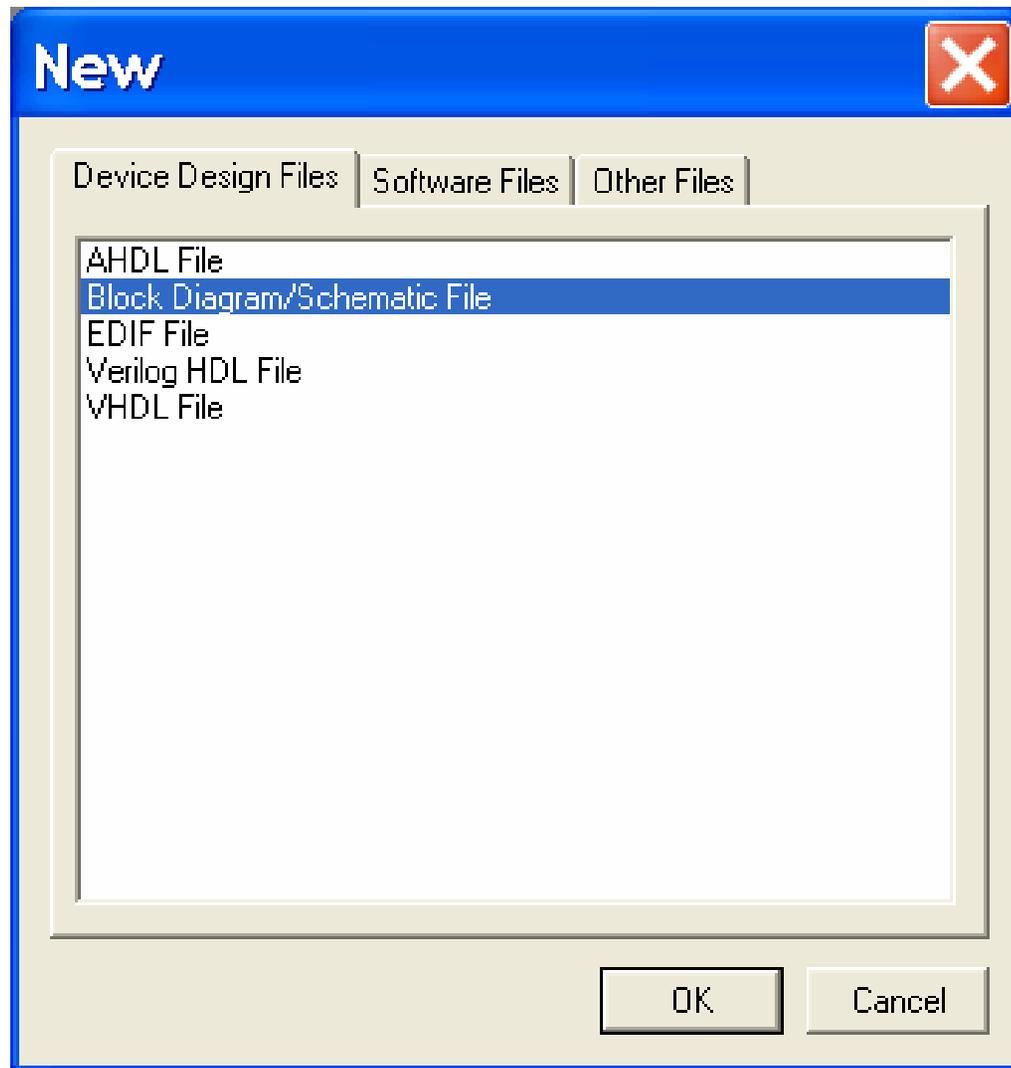
**Figure 1.5a and 1.5b.** Equivalent circuits for ORing active low inputs and outputs.



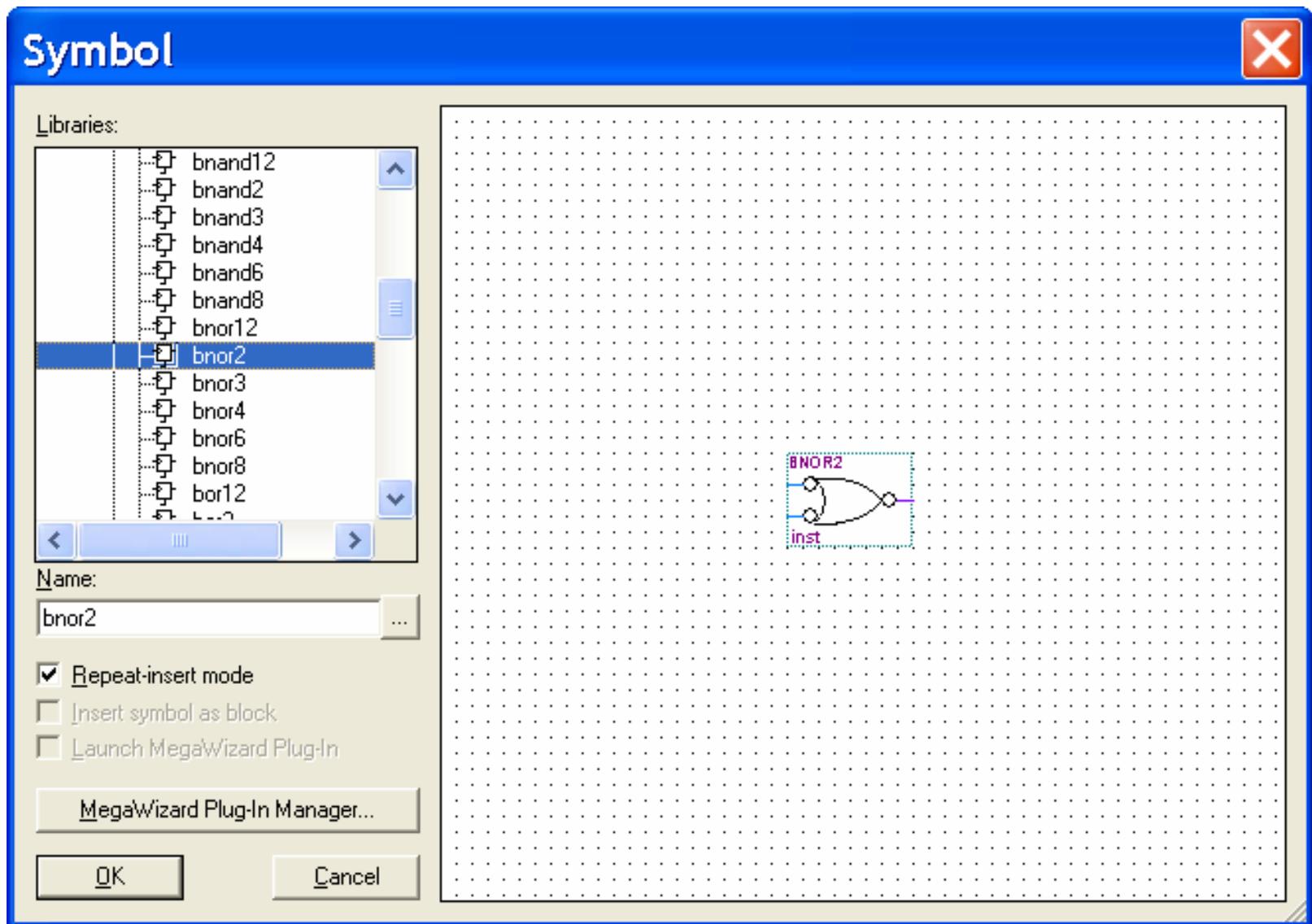
**Figure 1.6** Creating a new Quartus II Project.



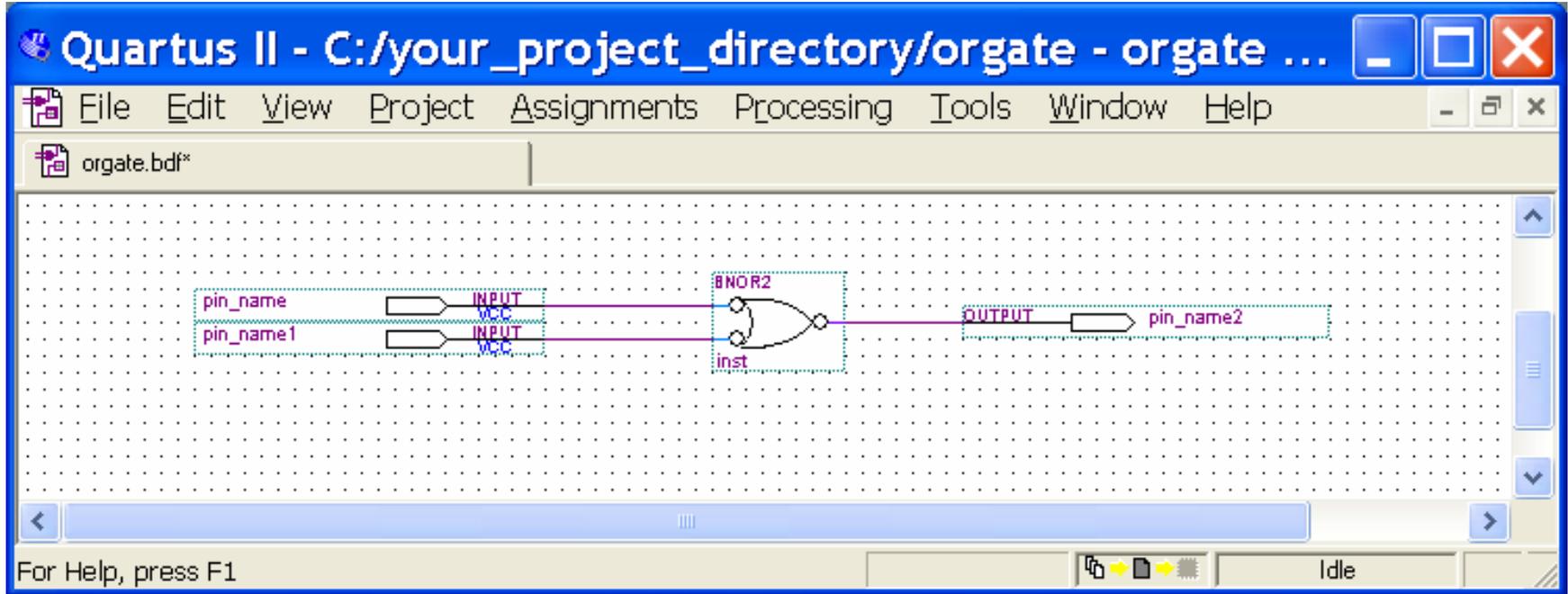
**Figure 1.7** Setting the FPGA Device Type.



**Figure 1.8** Creating the top-level project schematic design file.



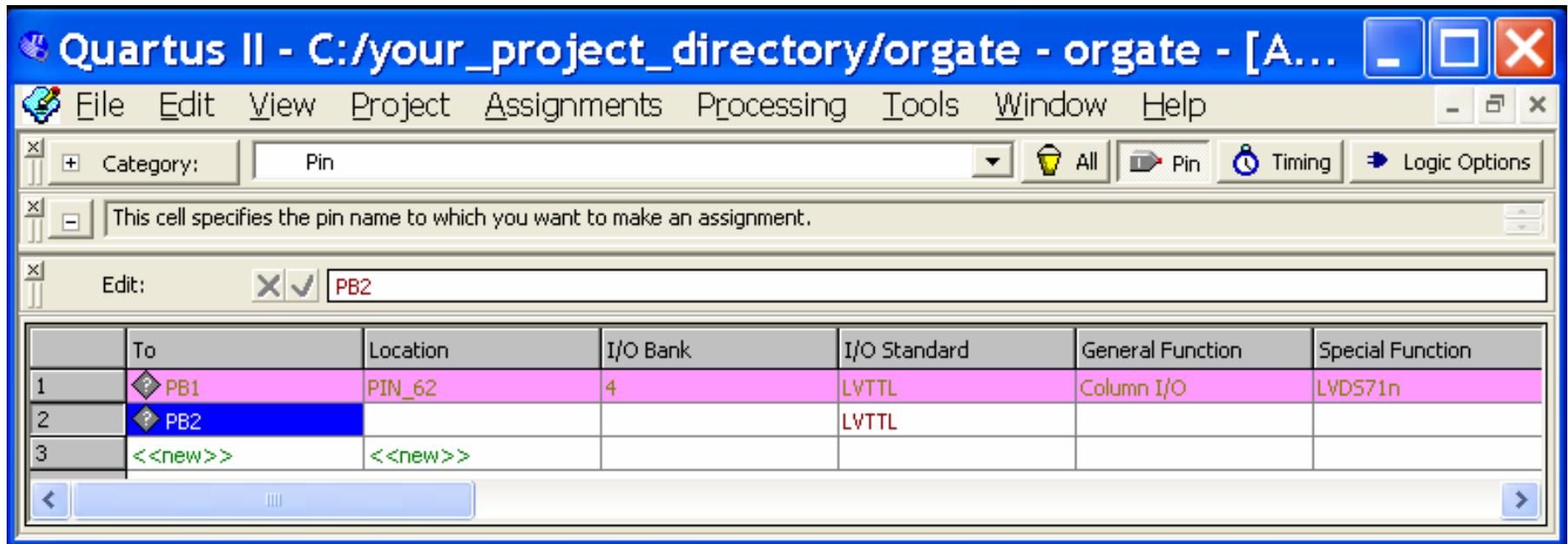
**Figure 1.9** Selecting a new symbol with the Symbol Tool.



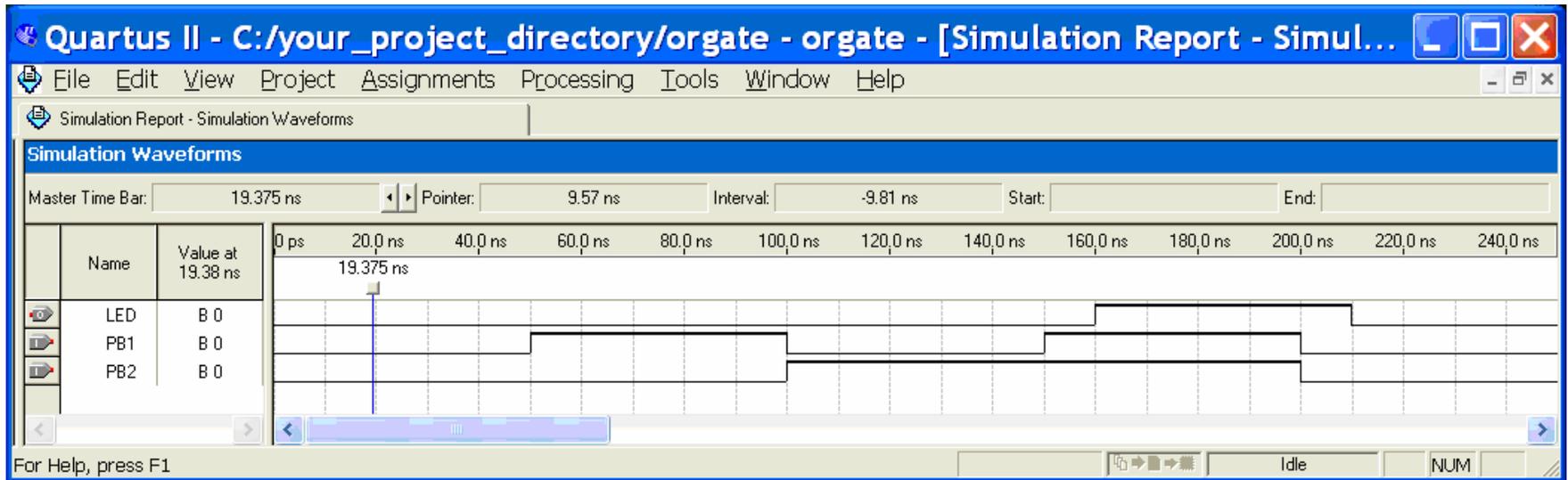
**Figure 1.10** Active low OR-gate schematic example with I/O pins connected.

Table 1.1 Hardwired connections on the FPGA chips for the design.

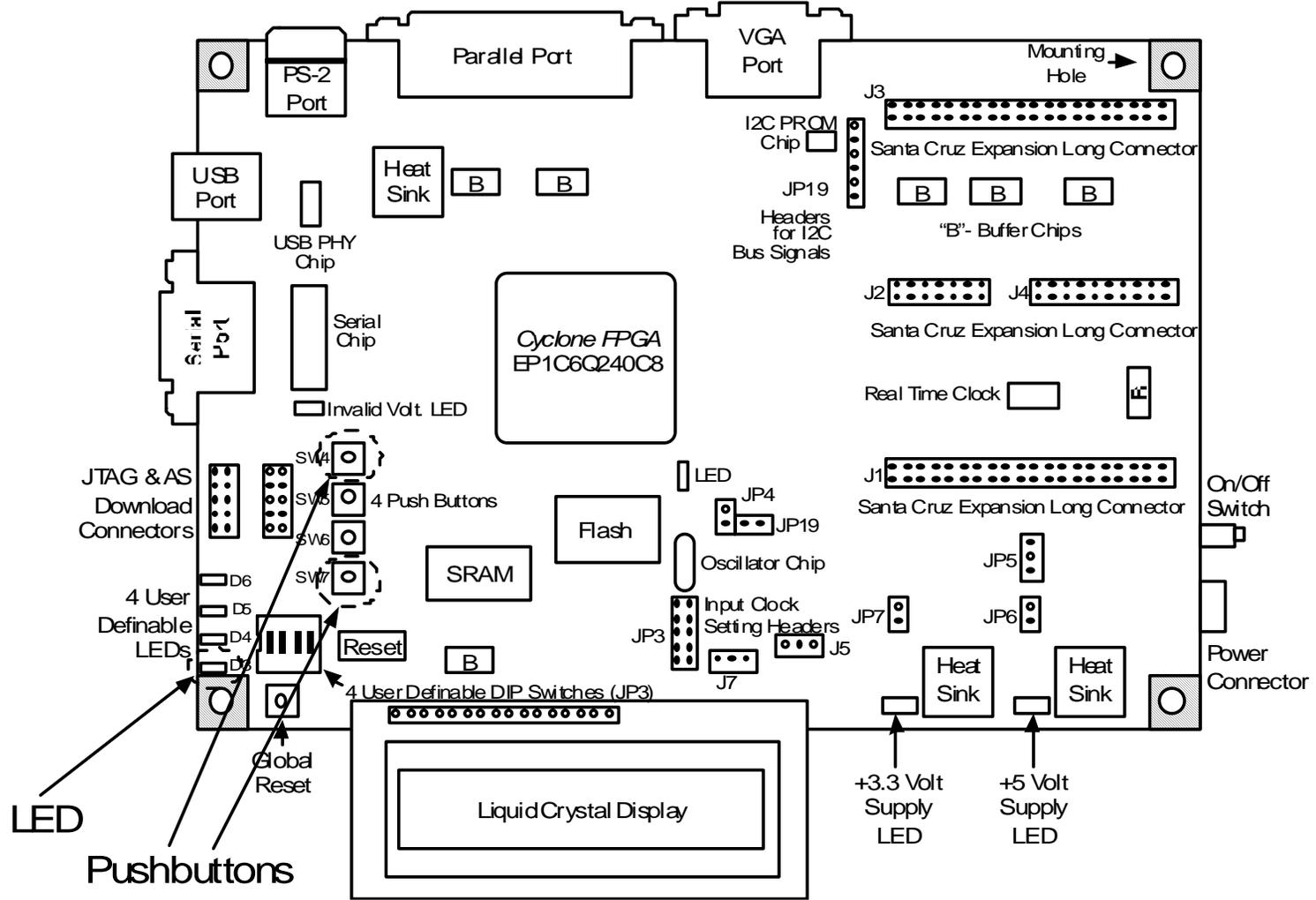
<b>I/O Device</b>	<b>UP 3 Pin Number Connections</b>	<b>UP 1 &amp; UP 2 Pin Number Connections</b>
PB1	62 (SW7)	28 (FLEX PB1)
PB2	48 (SW4)	29 (FLEX PB2)
LED	56 (D3)	14 (7Seg LED DEC. PT.)



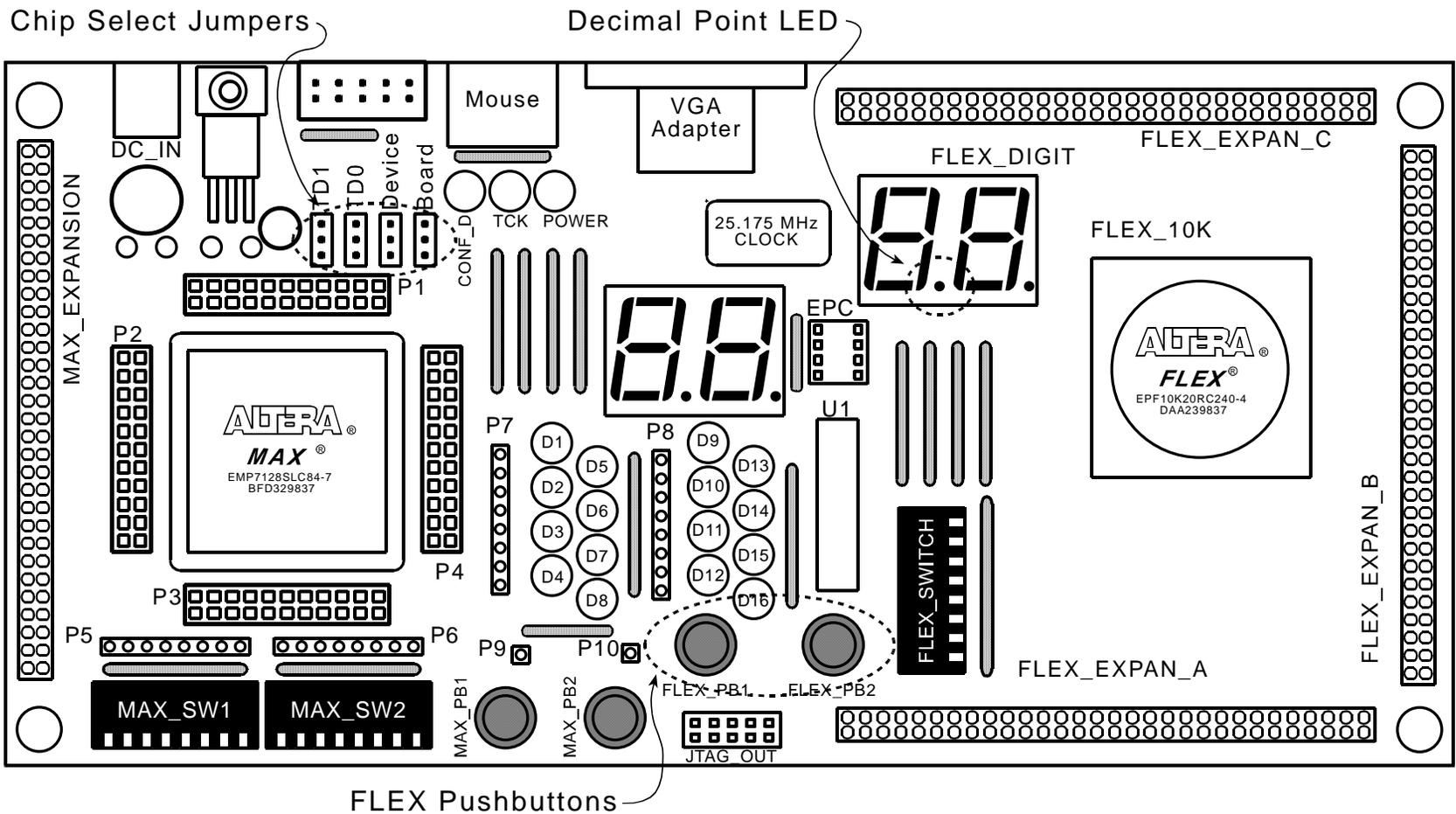
**Figure 1.11** Assigning Pins with the Assignment Editor.



**Figure 1.12** Active low OR-gate timing simulation with time delays.

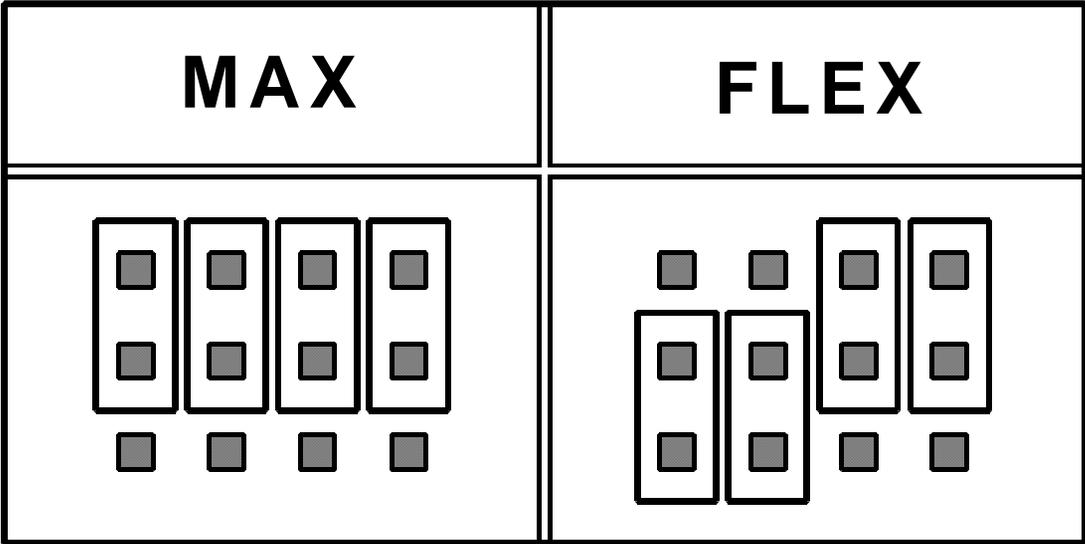


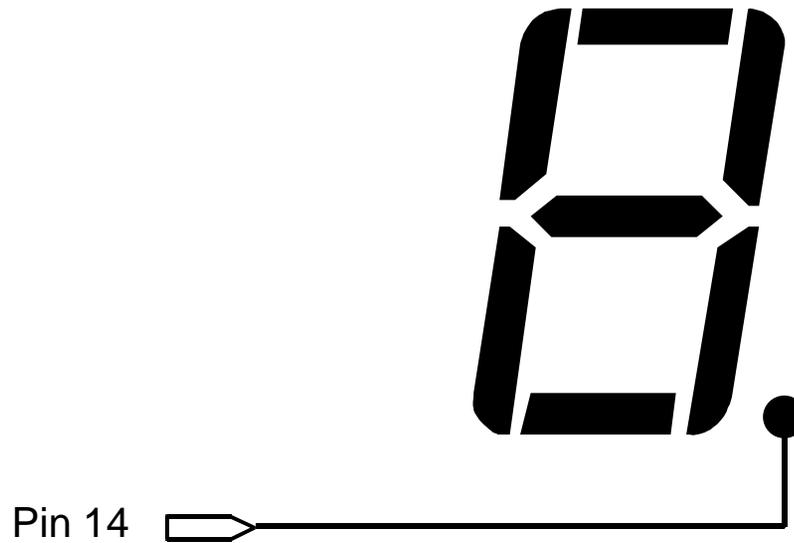
**Figure 1.13** ALTERA UP 3 board showing Pushbutton and LED locations used in design



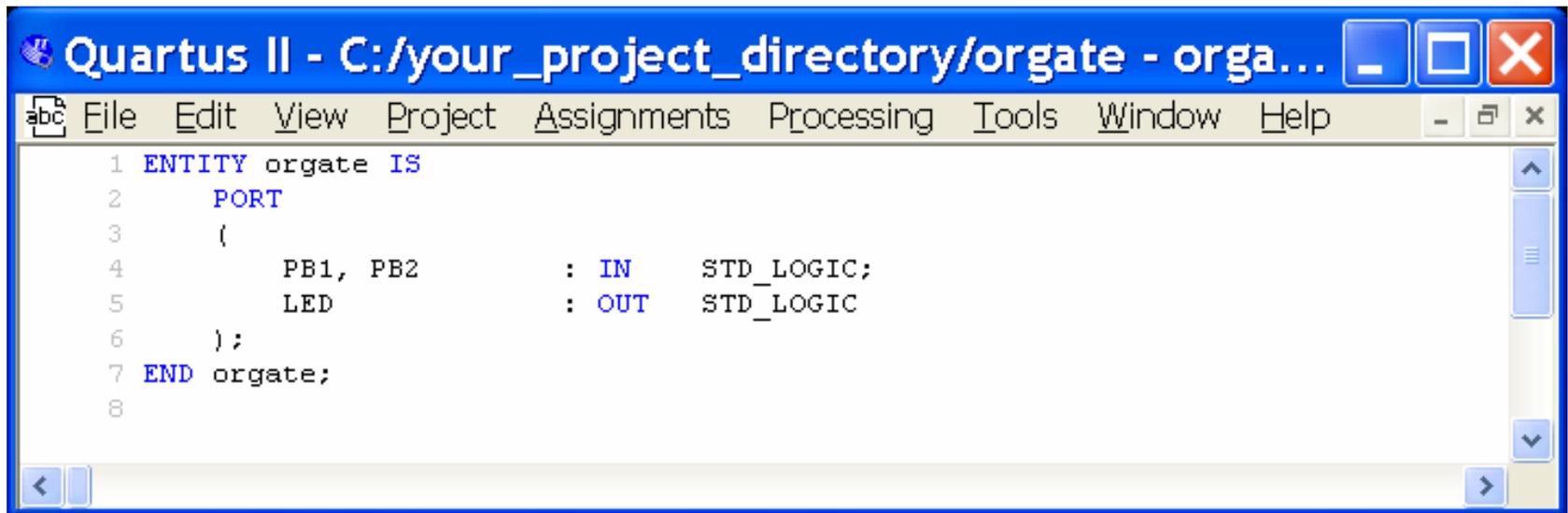
**Figure 1.14** ALTERA UP 2 board with jumper settings and PB1, PB2, and LED locations

Table 1.2 Jumper settings for downloading to the UP2 MAX and FLEX devices.





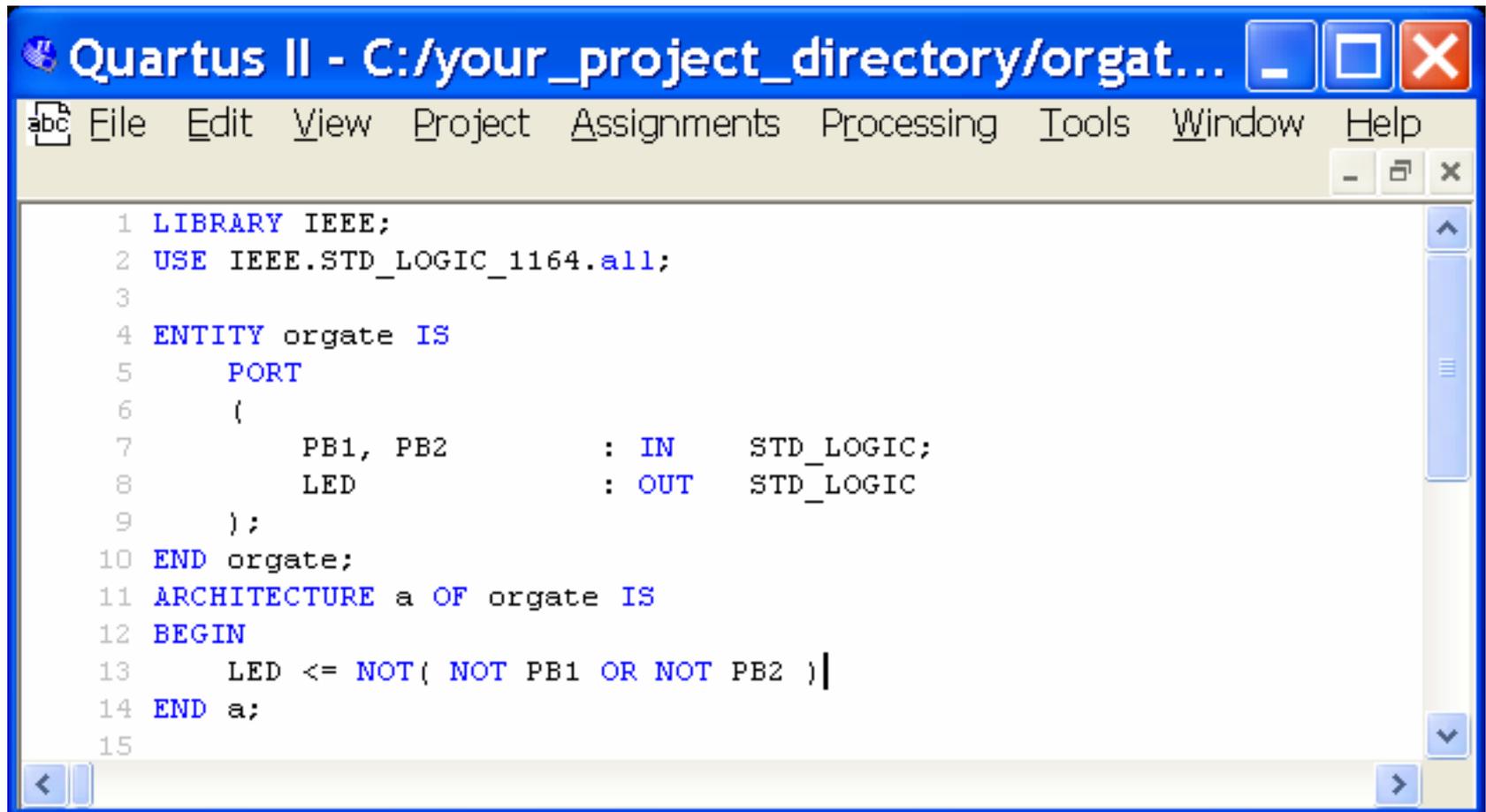
**Figure 1.15** UP 2's FLEX FPGA pin connection to seven-segment display decimal point.



The image shows a screenshot of the Quartus II software interface. The title bar reads "Quartus II - C:/your\_project\_directory/orgate - orga...". The menu bar includes "File", "Edit", "View", "Project", "Assignments", "Processing", "Tools", "Window", and "Help". The main text area contains the following VHDL code:

```
1 ENTITY orgate IS
2     PORT
3     (
4         PB1, PB2      : IN    STD_LOGIC;
5         LED           : OUT   STD_LOGIC
6     );
7 END orgate;
8
```

**Figure 1.16** VHDL Entity declaration text.

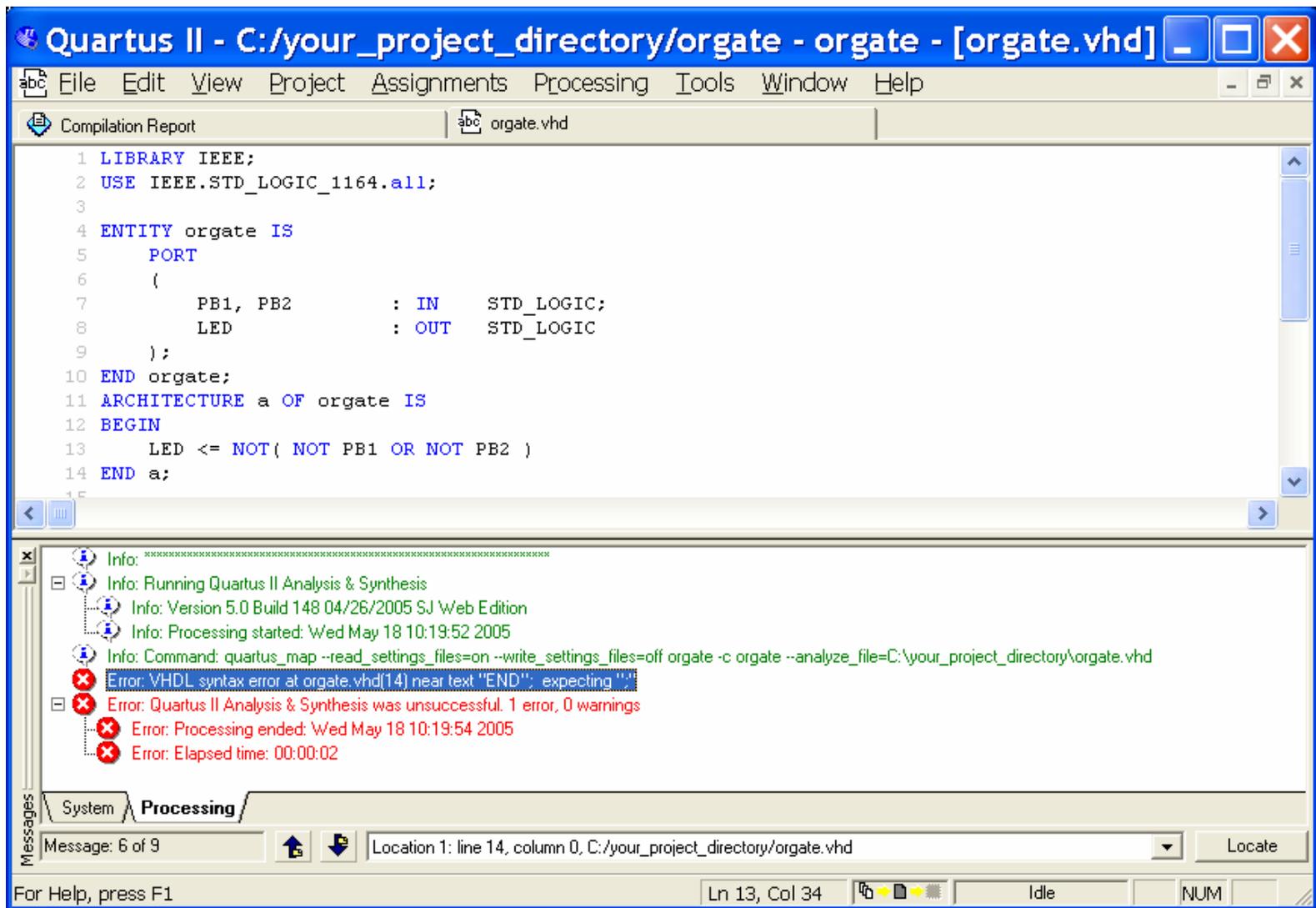


The image shows a screenshot of the Quartus II software interface. The title bar reads "Quartus II - C:/your\_project\_directory/orgat...". The menu bar includes "File", "Edit", "View", "Project", "Assignments", "Processing", "Tools", "Window", and "Help". The main editor window displays the following VHDL code:

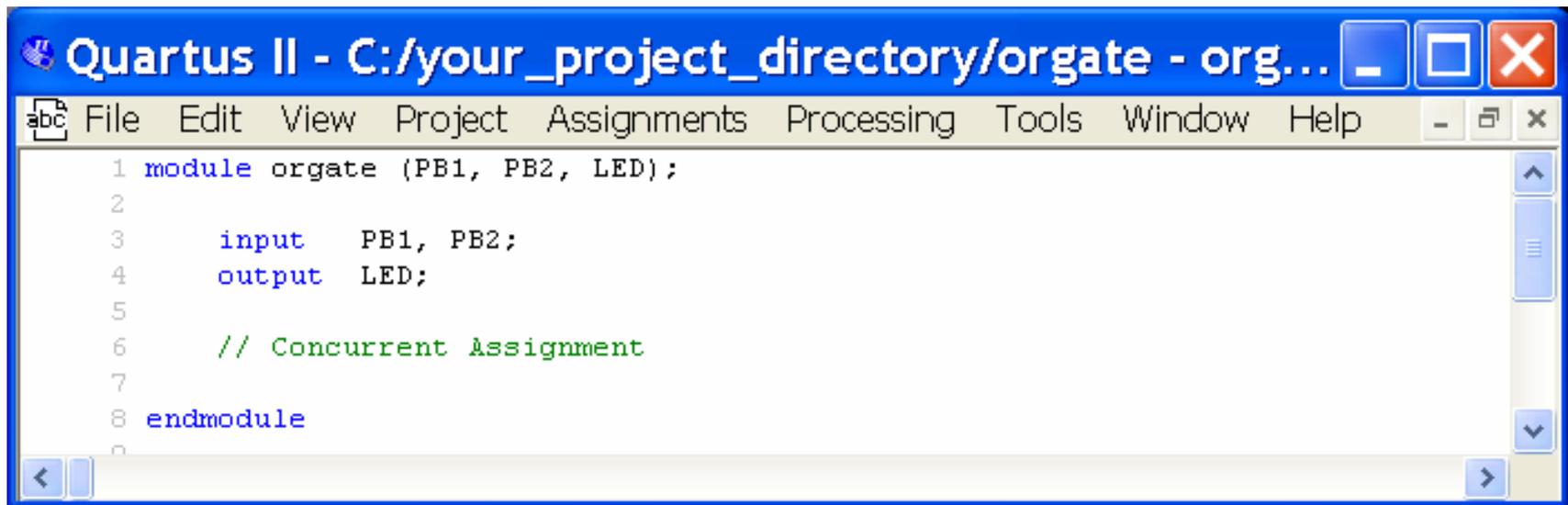
```
1 LIBRARY IEEE;
2 USE IEEE.STD_LOGIC_1164.all;
3
4 ENTITY orgate IS
5     PORT
6     (
7         PB1, PB2      : IN    STD_LOGIC;
8         LED           : OUT   STD_LOGIC
9     );
10 END orgate;
11 ARCHITECTURE a OF orgate IS
12 BEGIN
13     LED <= NOT( NOT PB1 OR NOT PB2 )|
14 END a;
15
```

The code defines an OR-gate entity named "orgate" with two input ports, PB1 and PB2, and one output port, LED. The architecture "a" implements the logic for the OR-gate. A syntax error is present on line 13, where the closing parenthesis of the NOT operator is missing, indicated by a vertical bar at the end of the line.

**Figure 1.17** VHDL OR-gate model (with syntax error).



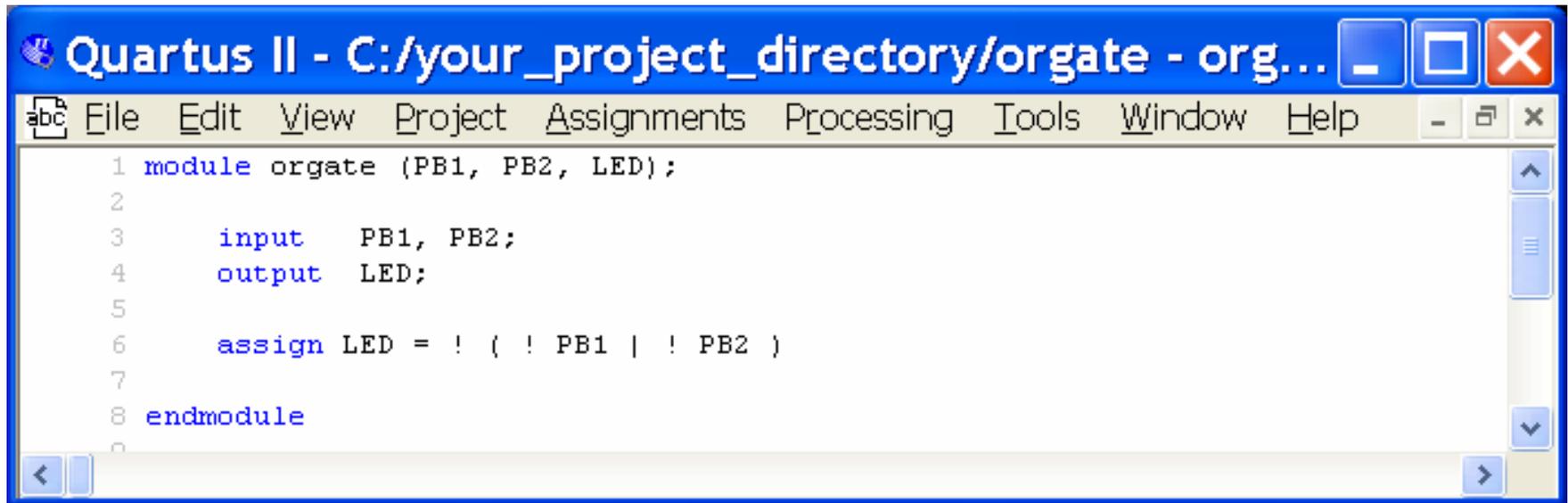
**Figure 1.18** VHDL compilation with a syntax error.

The image shows a screenshot of the Quartus II software interface. The title bar at the top reads "Quartus II - C:/your\_project\_directory/orgate - org...". Below the title bar is a menu bar with options: "File", "Edit", "View", "Project", "Assignments", "Processing", "Tools", "Window", and "Help". The main window displays a Verilog code editor with the following text:

```
1 module orgate (PB1, PB2, LED);  
2  
3     input    PB1, PB2;  
4     output  LED;  
5  
6     // Concurrent Assignment  
7  
8 endmodule  
9
```

The code is color-coded: "module", "input", "output", and "endmodule" are in blue; "PB1, PB2, LED" are in black; and "// Concurrent Assignment" is in green. The editor has a scroll bar on the right and a line number column on the left.

**Figure 1.19** Verilog module declaration text.

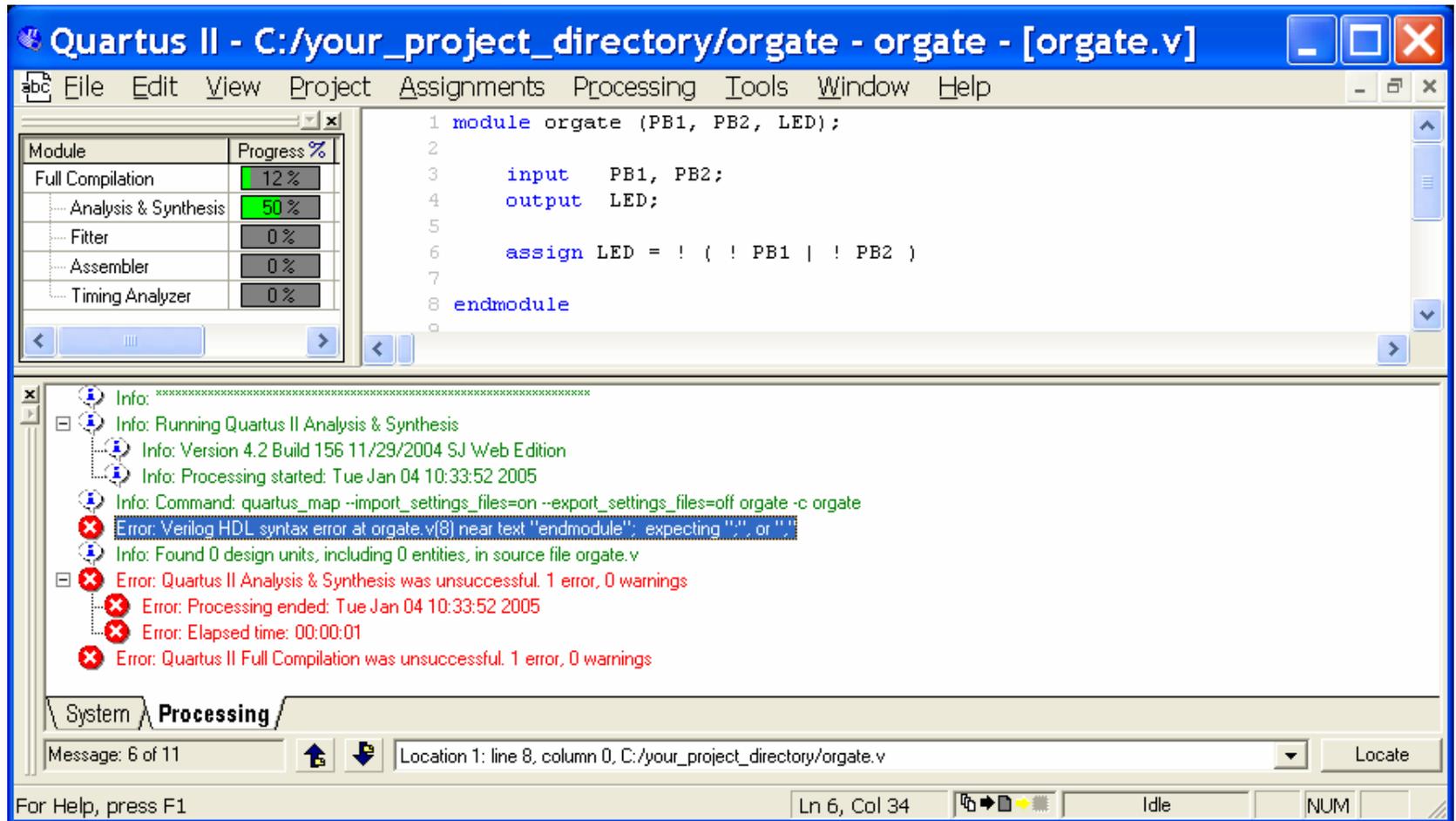


The image shows a screenshot of the Quartus II software interface. The title bar reads "Quartus II - C:/your\_project\_directory/orgate - org...". The menu bar includes "File", "Edit", "View", "Project", "Assignments", "Processing", "Tools", "Window", and "Help". The main text area contains the following Verilog code:

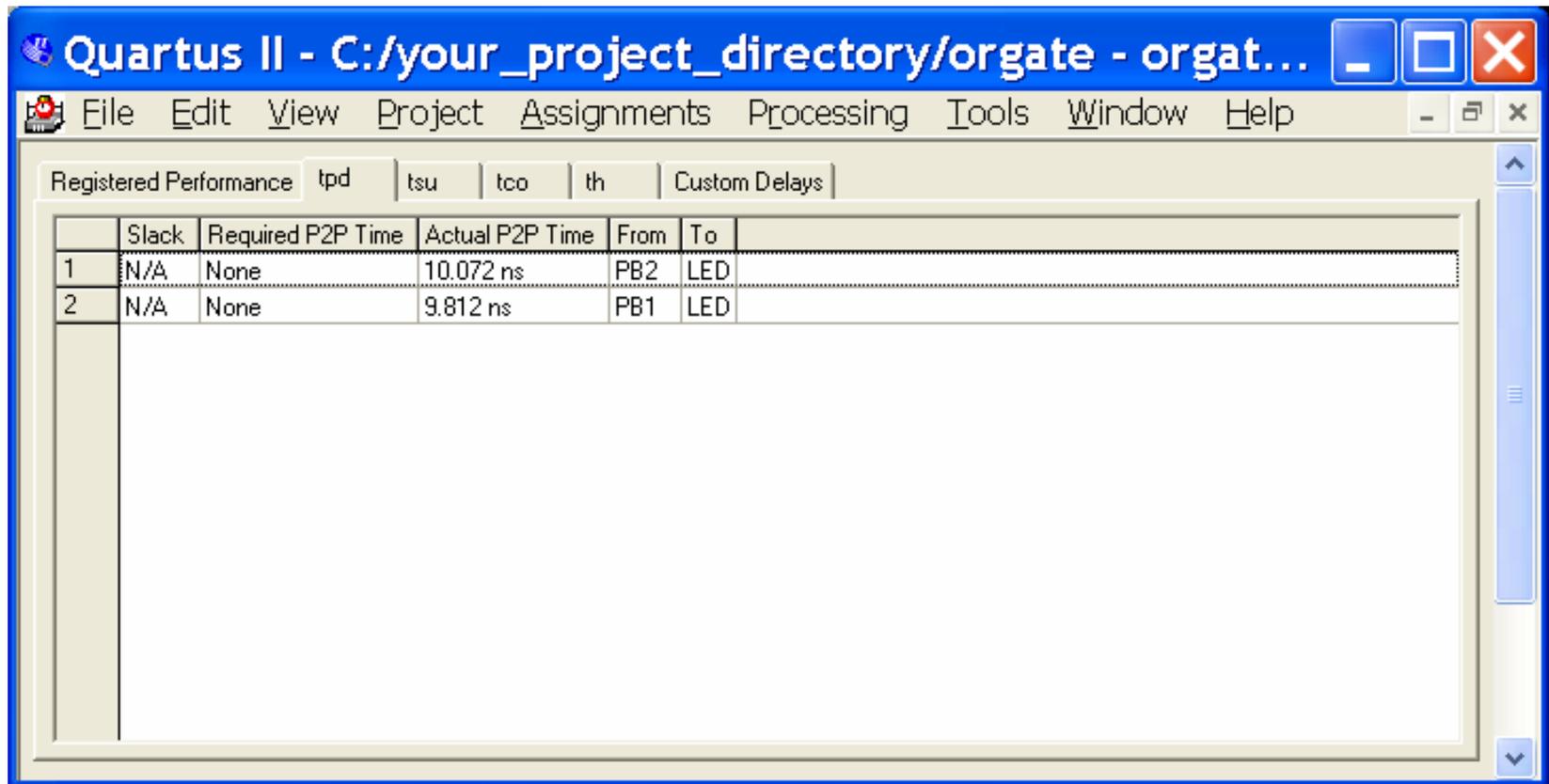
```
1 module orgate (PB1, PB2, LED);  
2  
3     input    PB1, PB2;  
4     output  LED;  
5  
6     assign LED = ! ( ! PB1 | ! PB2 )  
7  
8 endmodule  
9
```

The code defines a module named "orgate" with two inputs, PB1 and PB2, and one output, LED. The logic is implemented using an "assign" statement: LED = ! ( ! PB1 | ! PB2 ). There is a syntax error in the expression " ! PB1 | ! PB2 " because the OR operator "|" is not valid in Verilog; the correct operator is "||".

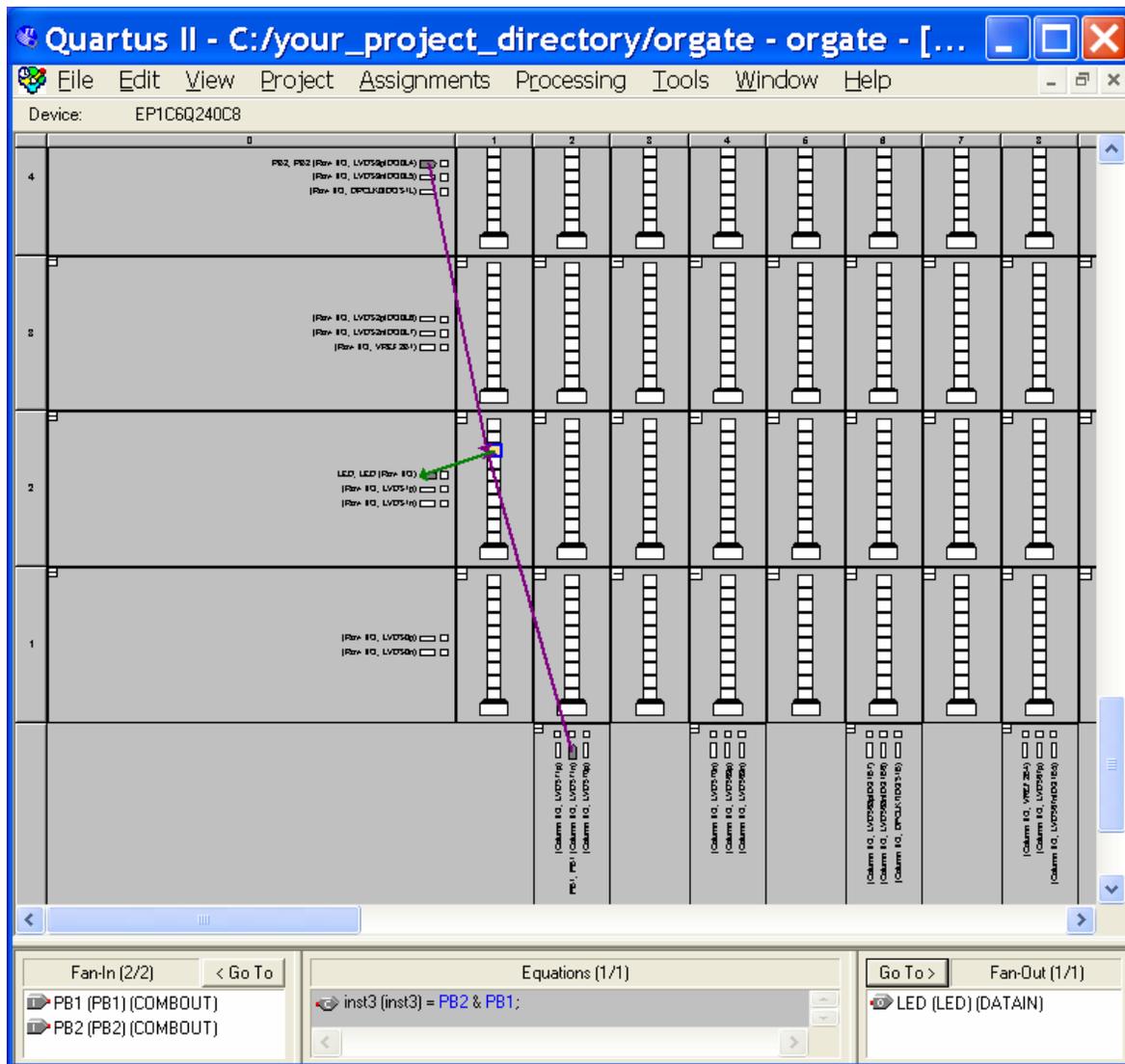
**Figure 1.20** Verilog active low OR-gate model (with syntax error).



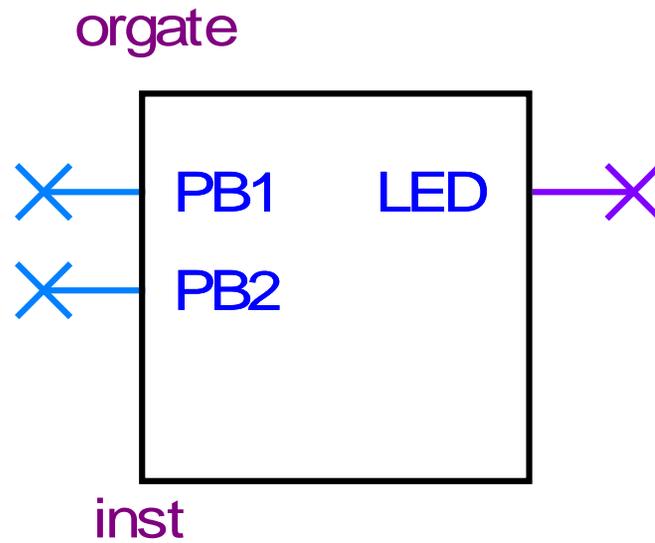
**Figure 1.21** Verilog compilation with a syntax error.



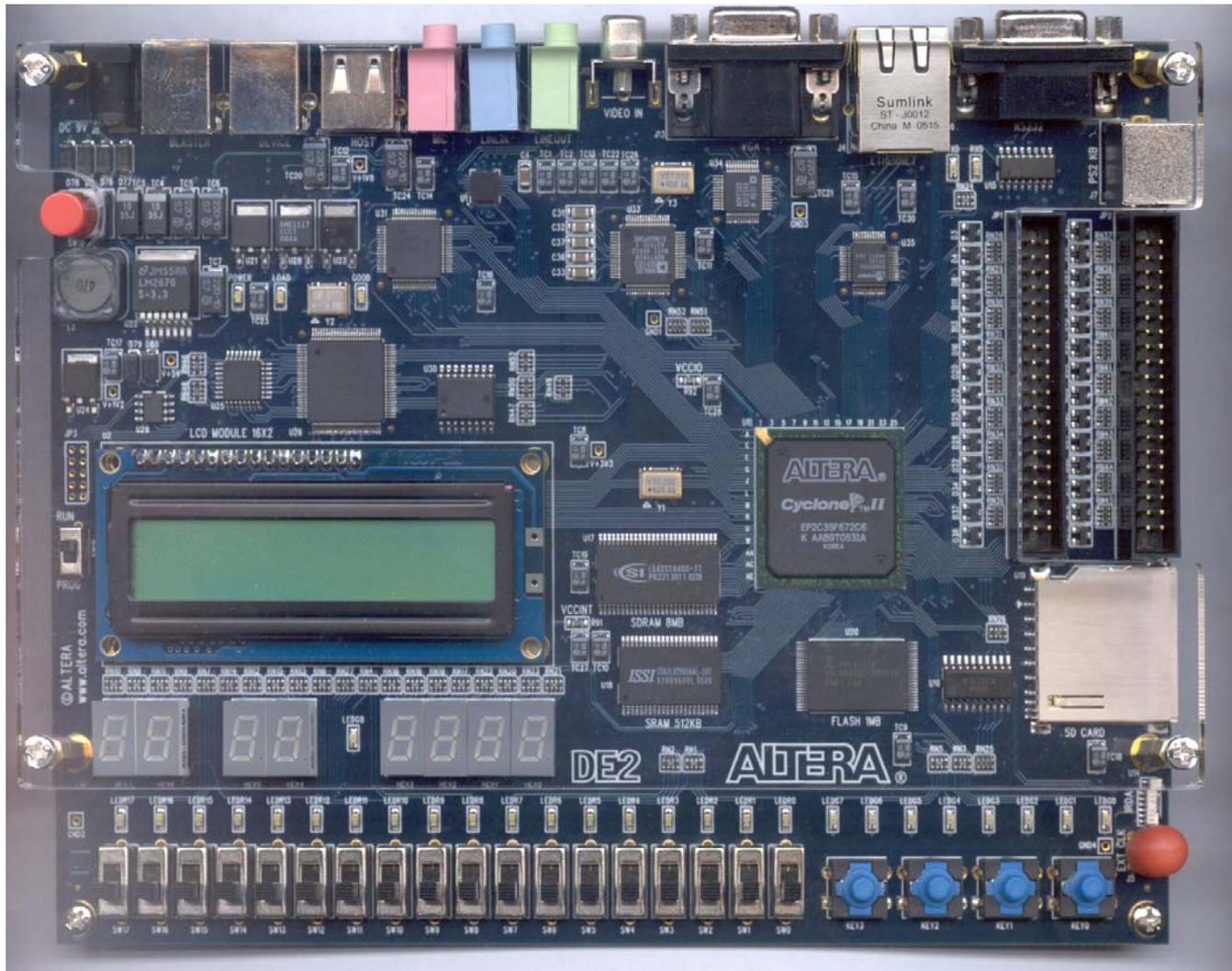
**Figure 1.22** Timing analyzer showing input to output timing delays.



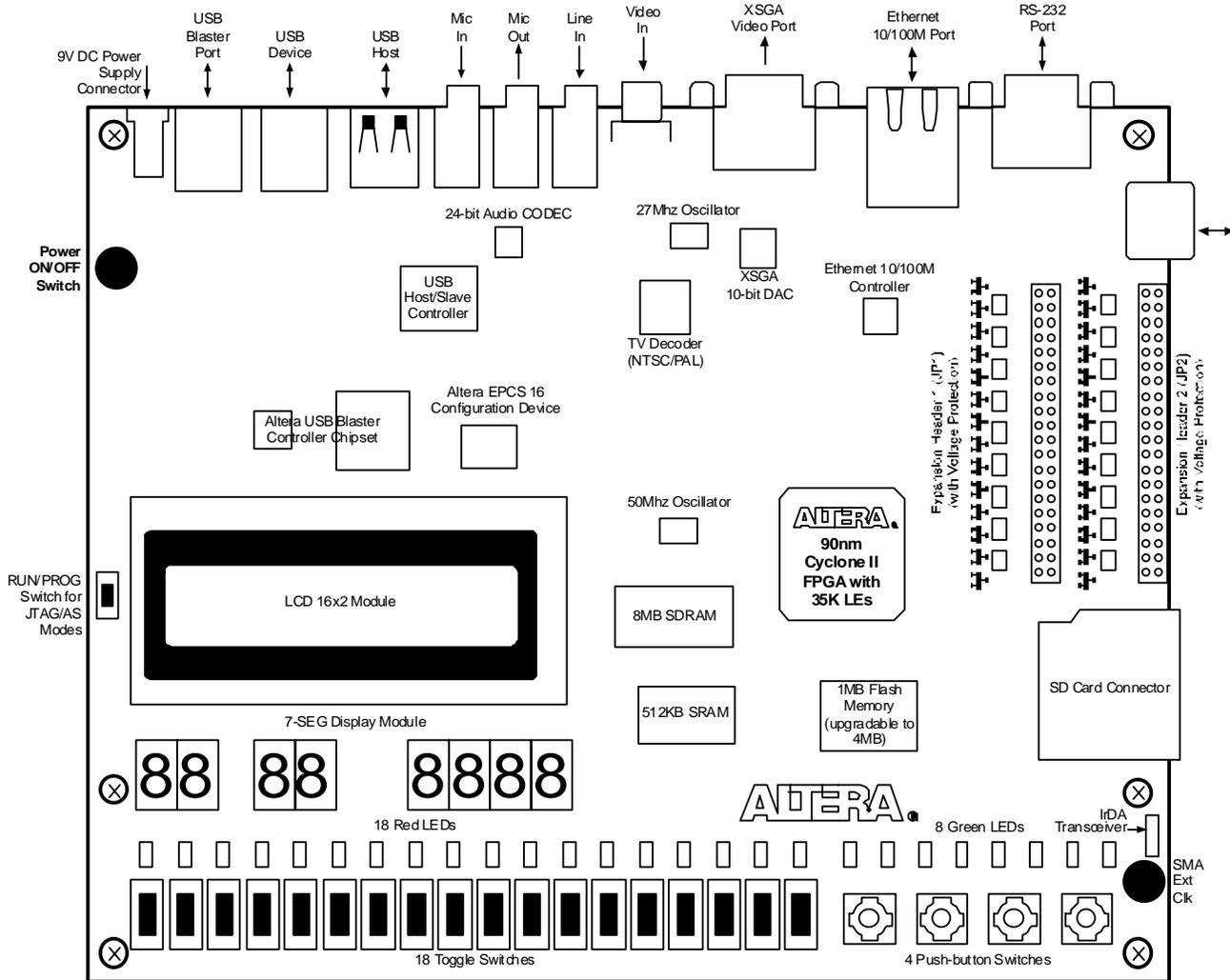
**Figure 1.23** Floorplan view showing internal FPGA placement of OR-gate in LE and I/O pins



**Figure 1.24** ORgate design symbol.



**Figure 1.14** The Altera DE2 FPGA Development board



**Figure 1.15** The Altera DE2 FPGA Development board