

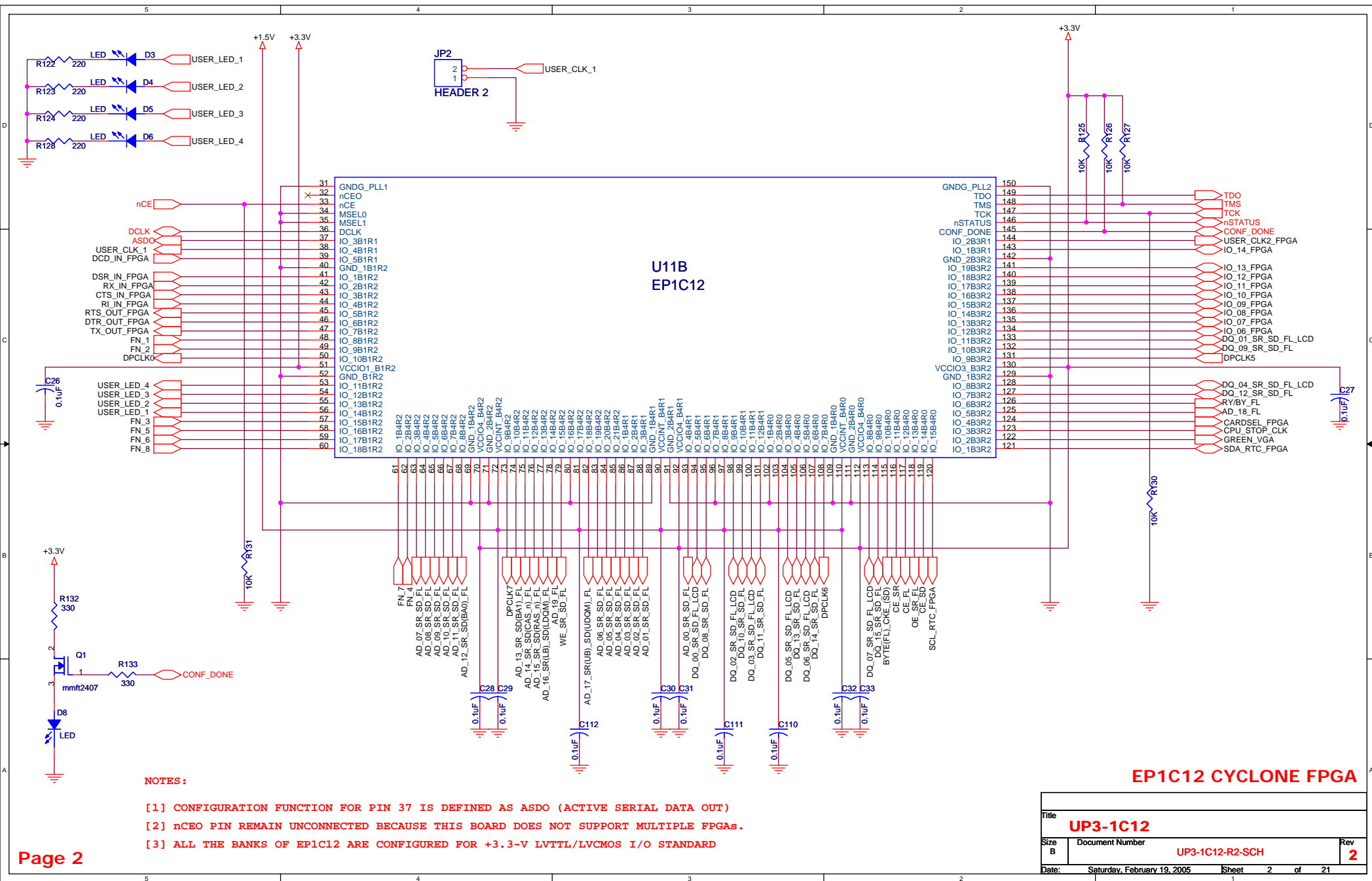


# UP3-1C12 Schematic

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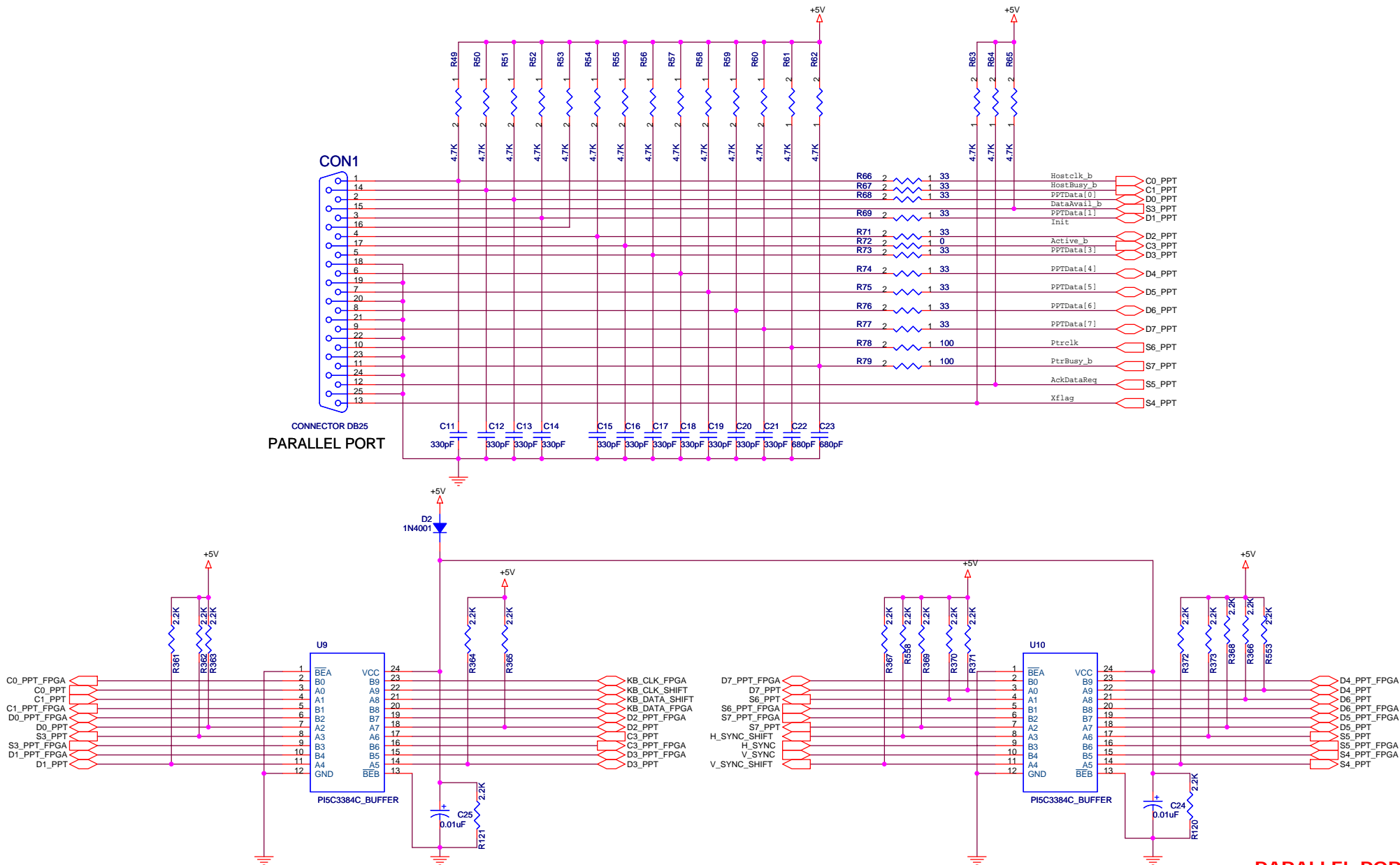
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CON1  
PARALLEL PORT

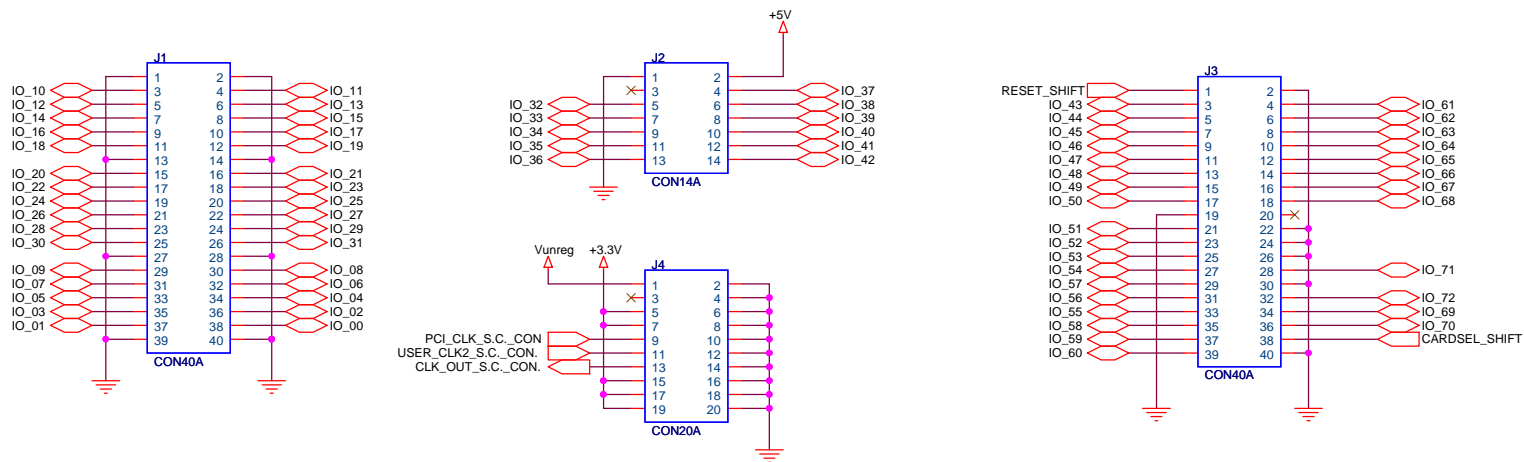


# NOTES:

- [1] C2\_PPT\_SIGNAL OF PARALLEL PORT REMAINS OPEN ON THIS BOARD (NOT CONNECTED TO ANY FPGA PIN)  
- IT IS JUST PULLED HIGH AT +5V AT PPT CONNECTOR
- [2] IF +5V LOGIC LEVEL IS REQUIRED FOR V\_SYNC\_SHIFT & H\_SYNC\_SHIFT SIGNALS THEN STUFF PULL UP RESISTORS R367 & R558, OTHERWISE DON'T

PARALLEL PORT

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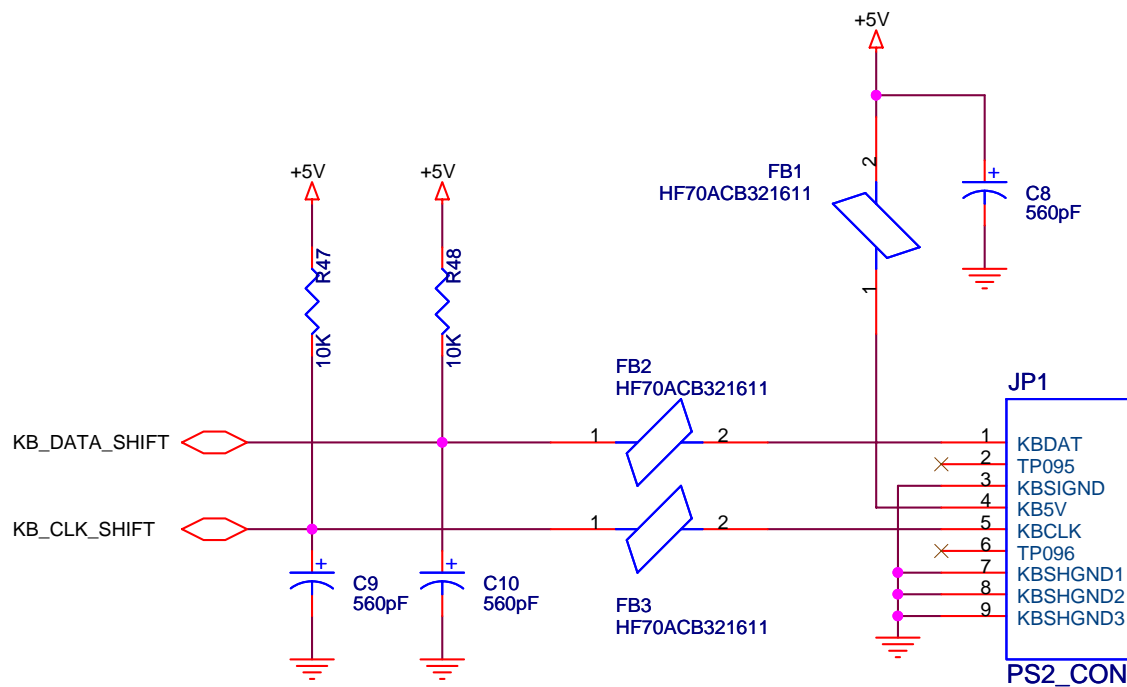


#### NOTES:

- [1] PCICLK\_OUT (33.3MHz) FOR SNAP IN BOARD IS PROVIDED FORM CLOCK CHIP (PI6C106)
- [2] J3.34 IS USED AS A PROTO I/O ACCORDING TO THE NIOS BOARD SCHEMATICS
- [3] FOR LEVELSHIFTING, SEE PAGE\_10\_L.S.S.C.CONN.

#### SANTA CRUZ CONNECTOR

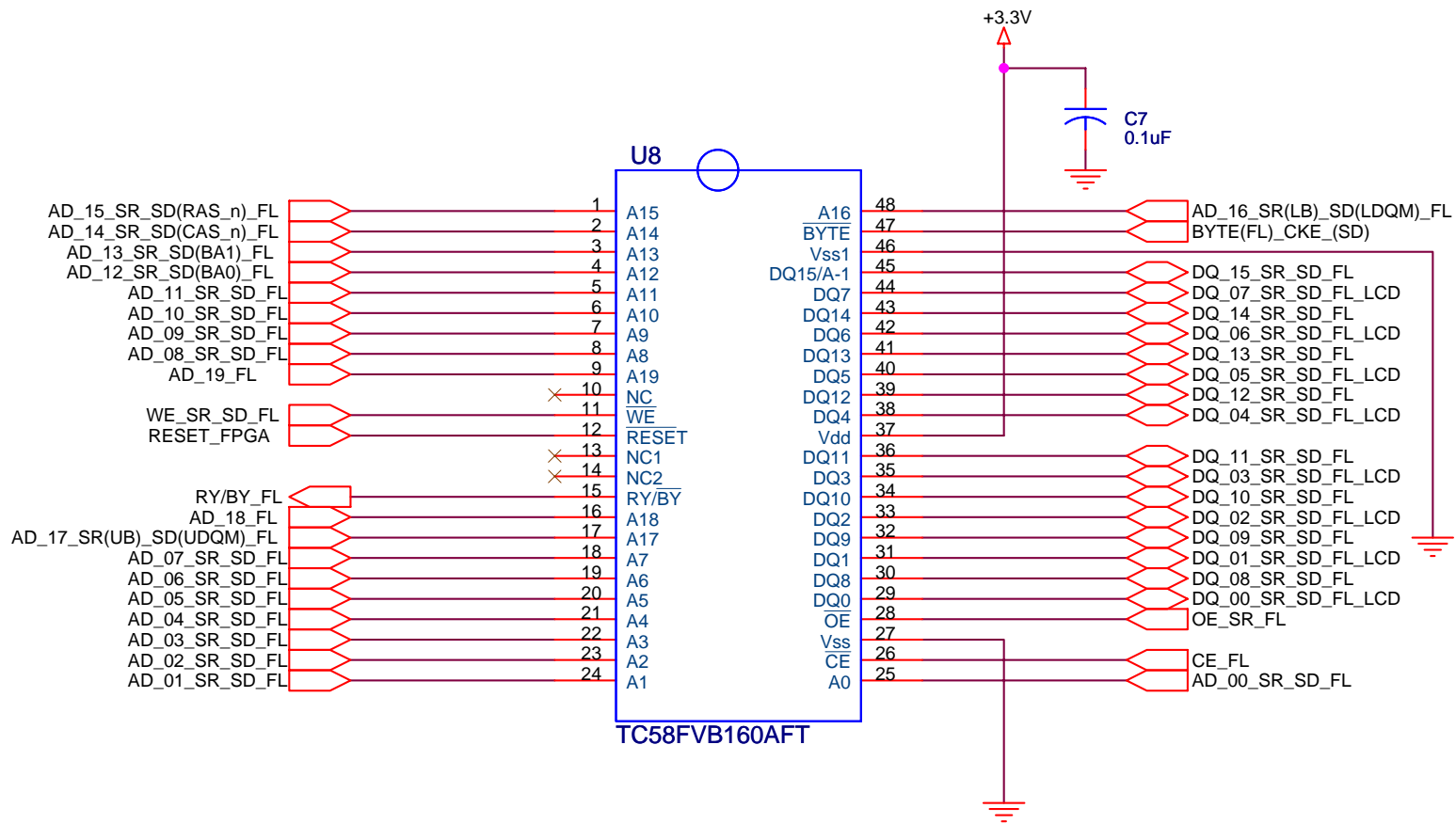
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**NOTE: FOR LEVEL SHIFTING, SEE PAGE3\_PPT**

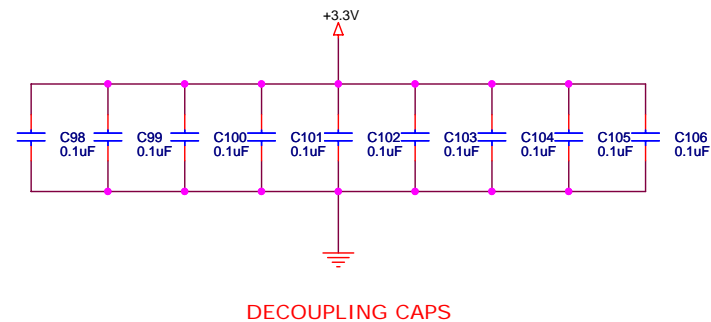
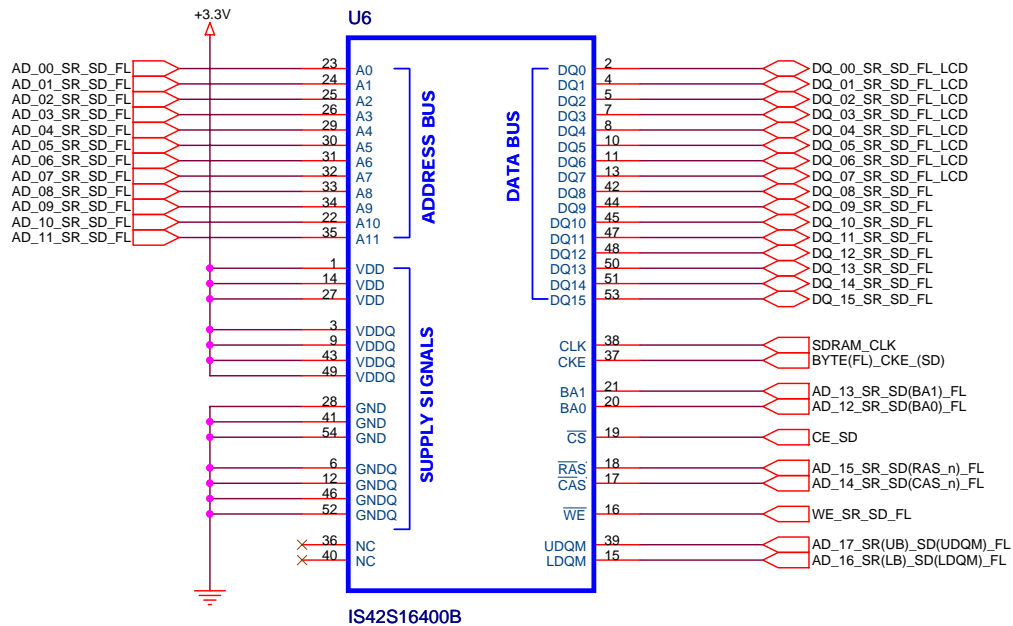
## PS/2 CONNECTOR

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**CMOS FLASH**

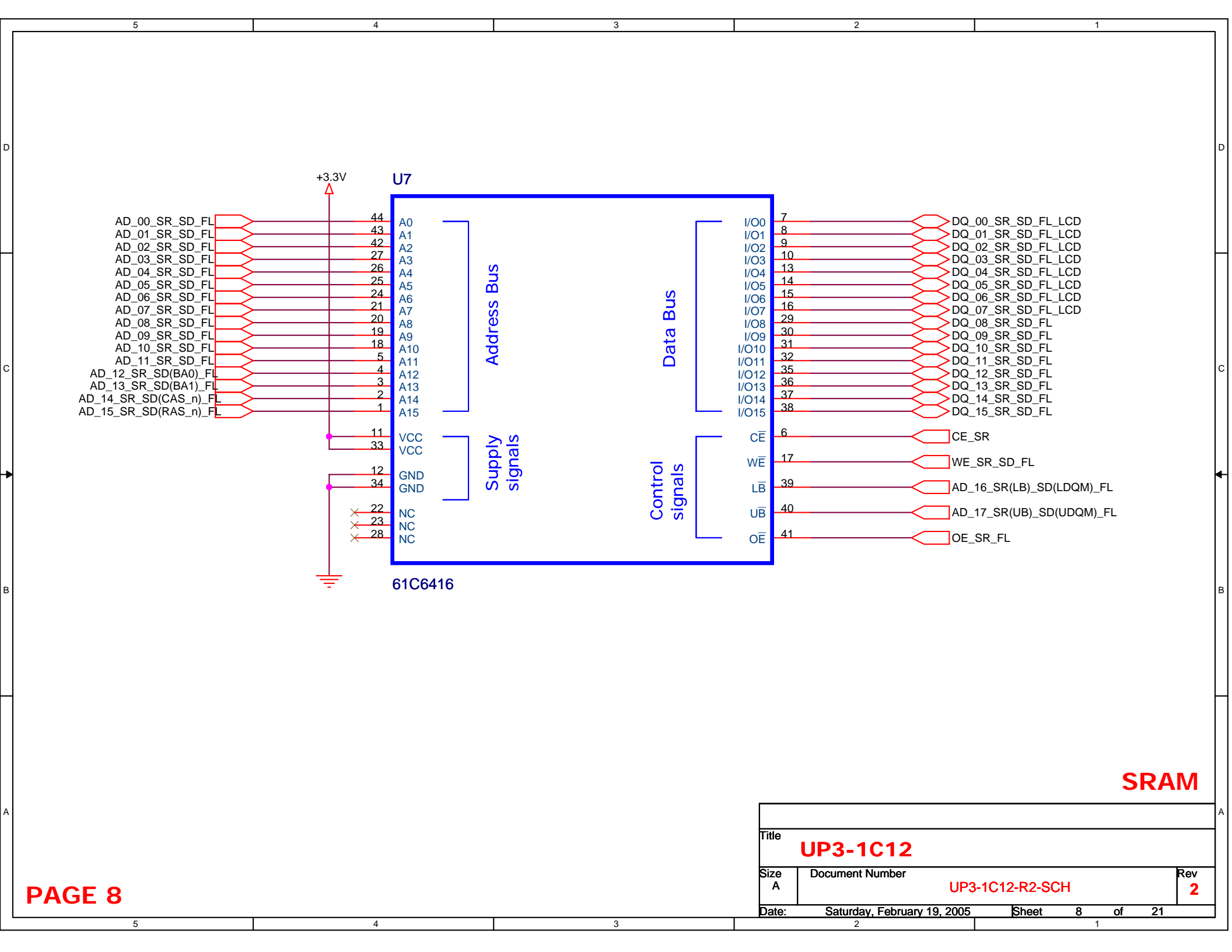
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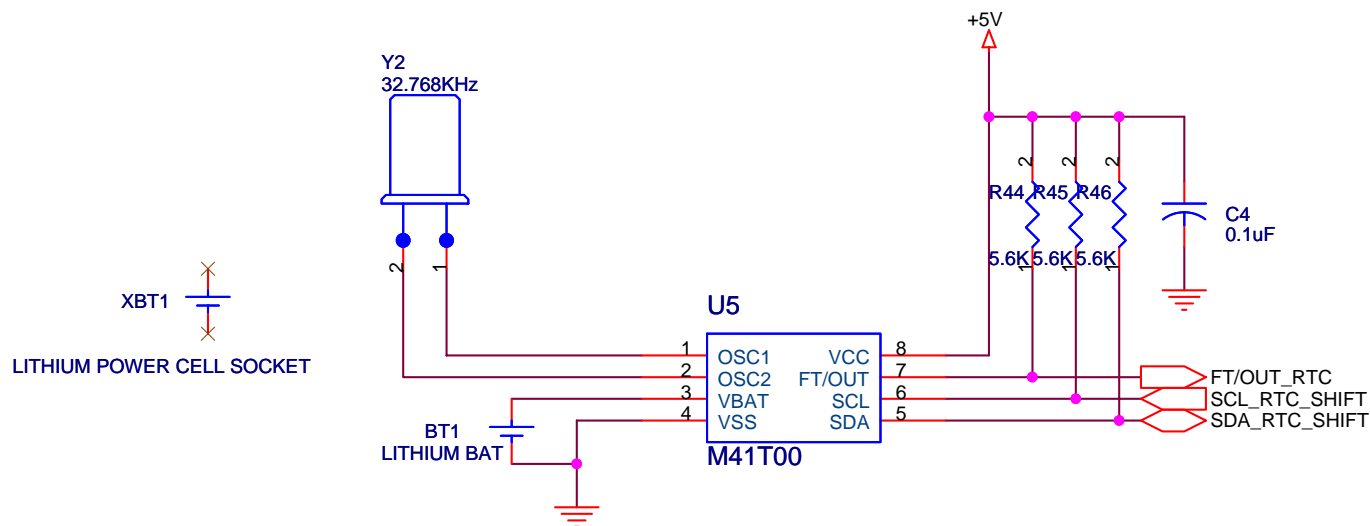
**CMOS SDRAM**

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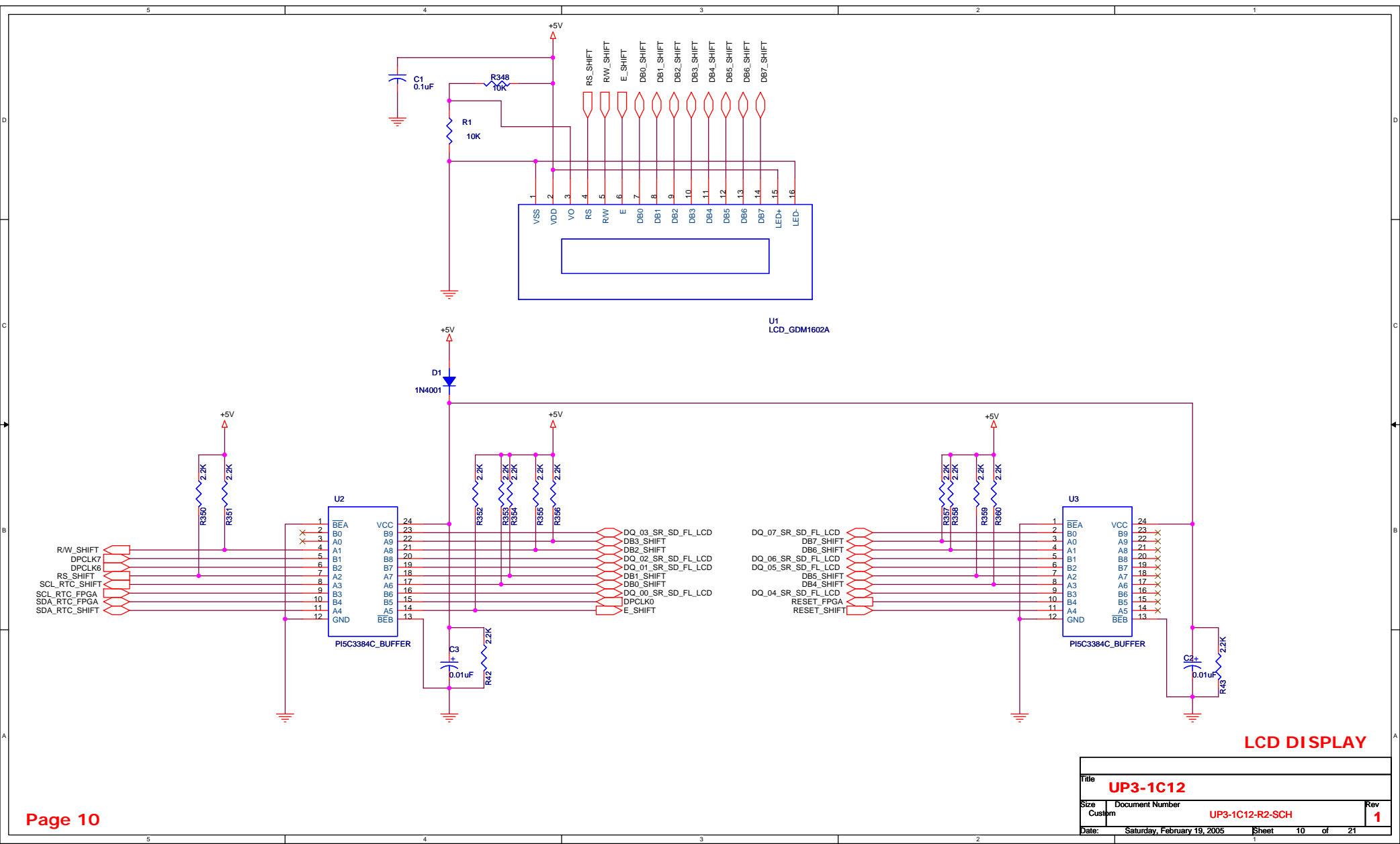
# NOTES:

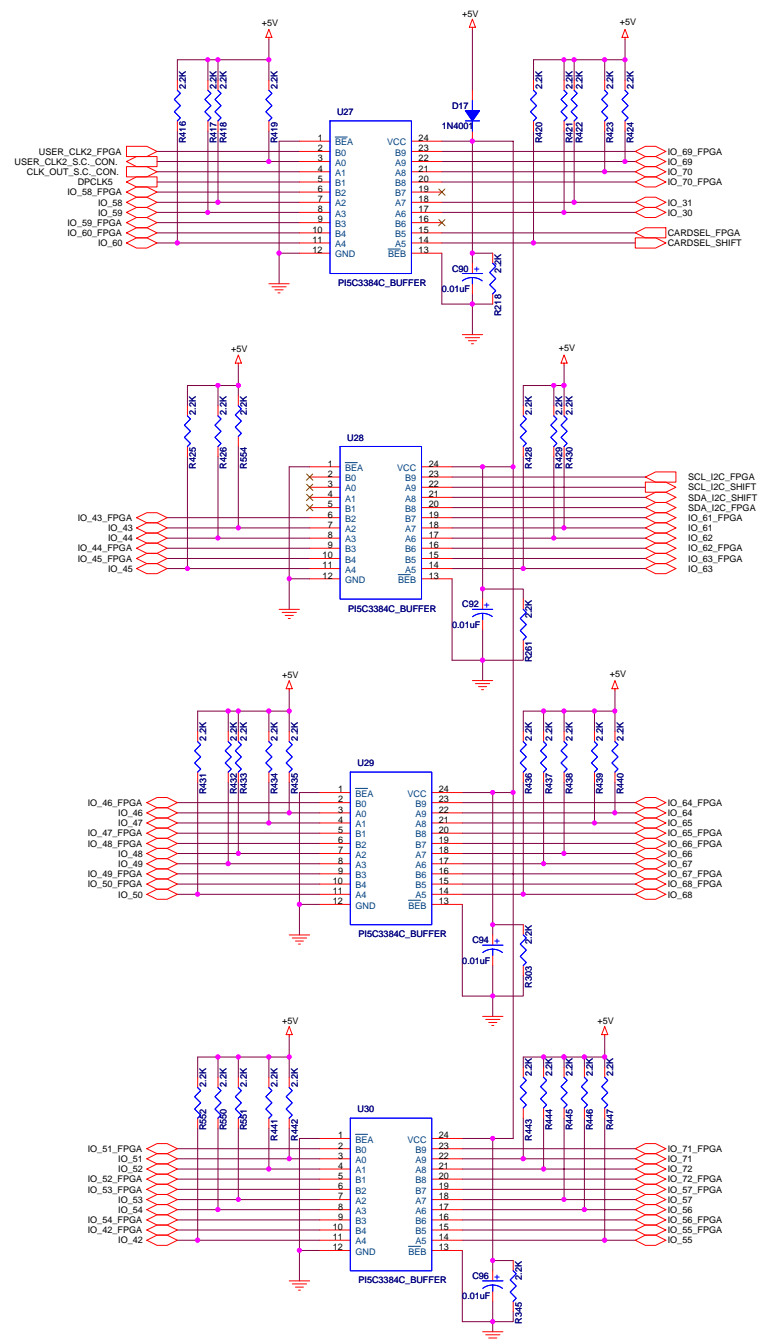
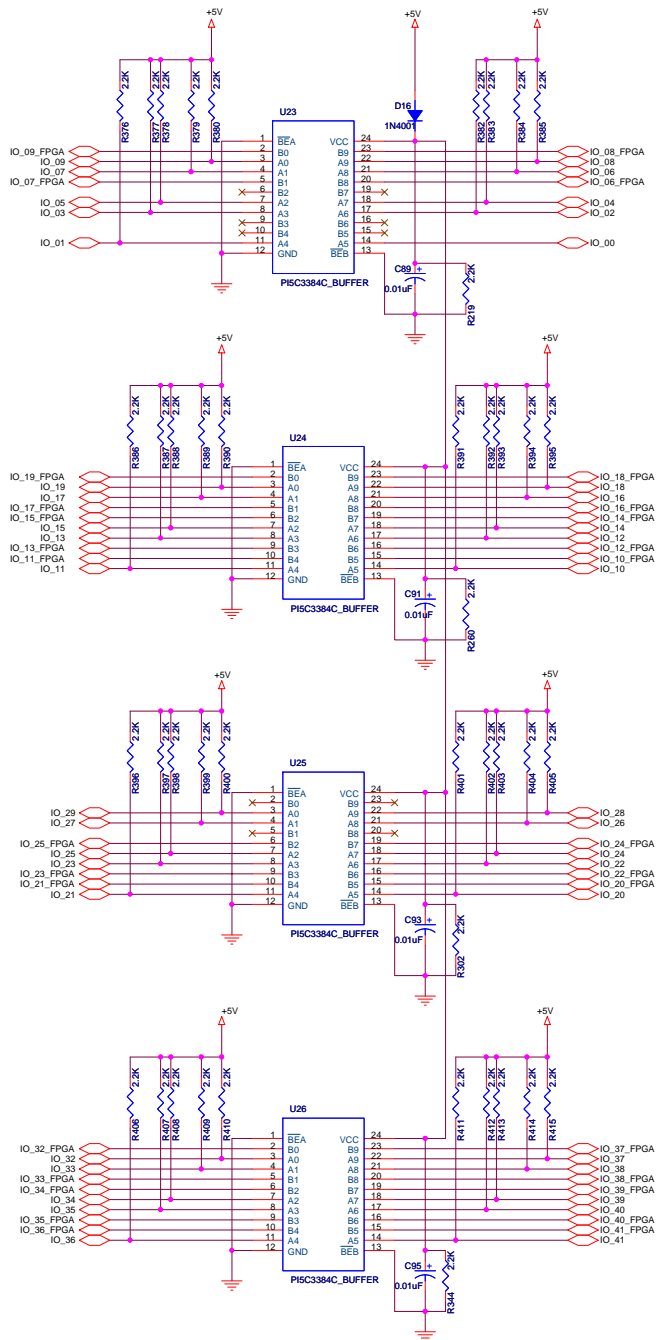
[1] FOR LEVEL SHIFTING, SEE PAGE9\_LCD\_DISPLAY

[2] BATTERY SOCKET IS USED FOR Li BATTERY (BT1)

I2C RTS

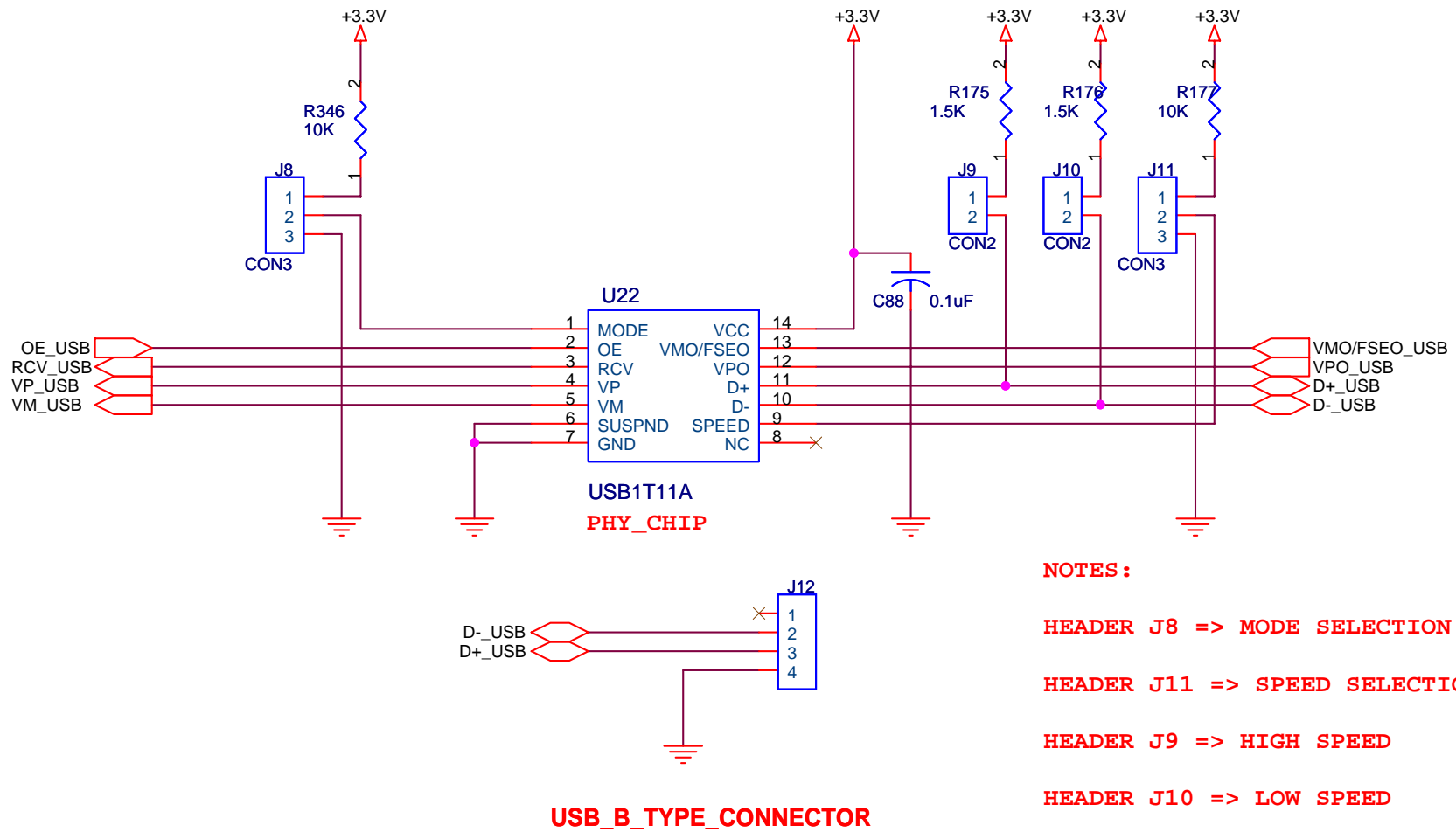
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## LEVEL SHIFTERS FOR SANTA CRUZ CONNECTOR

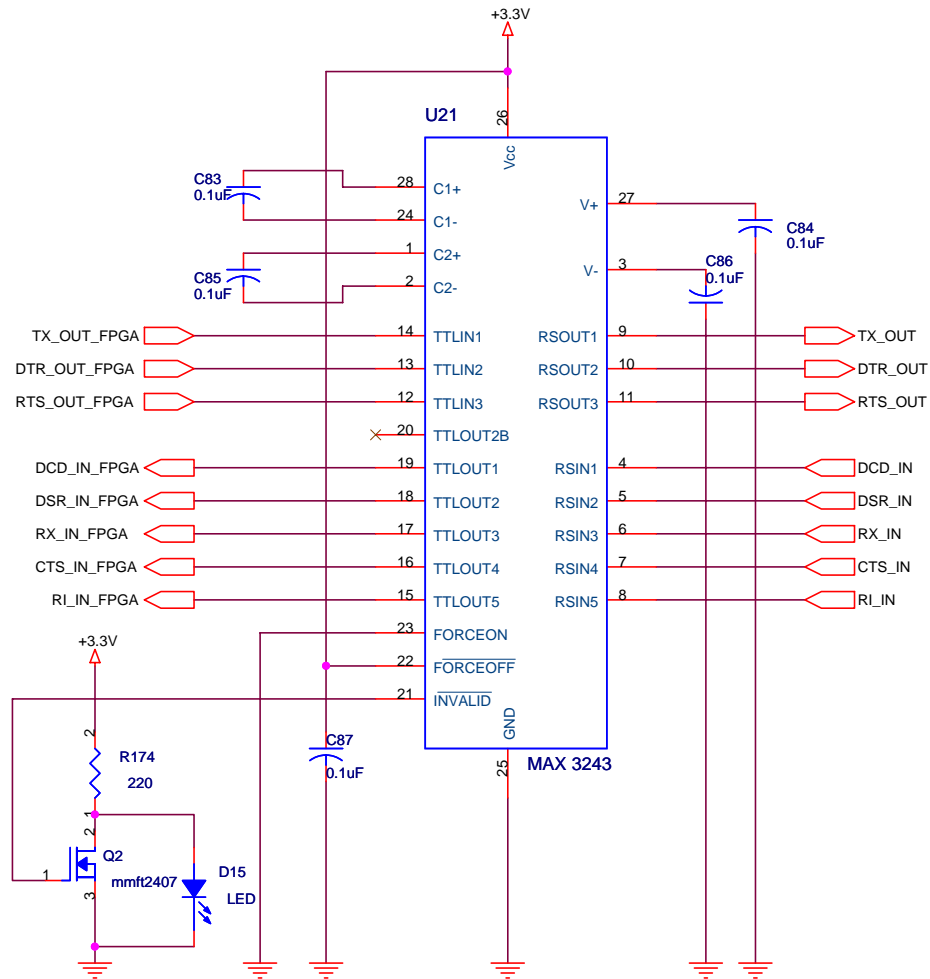
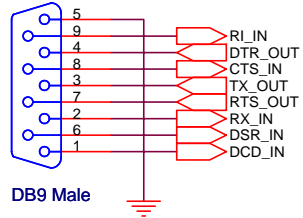
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## USB PHY CHIP & USB B TYPE CONNECTOR

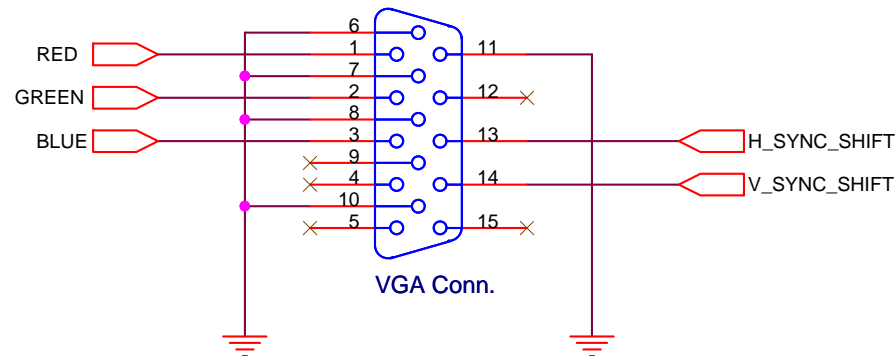
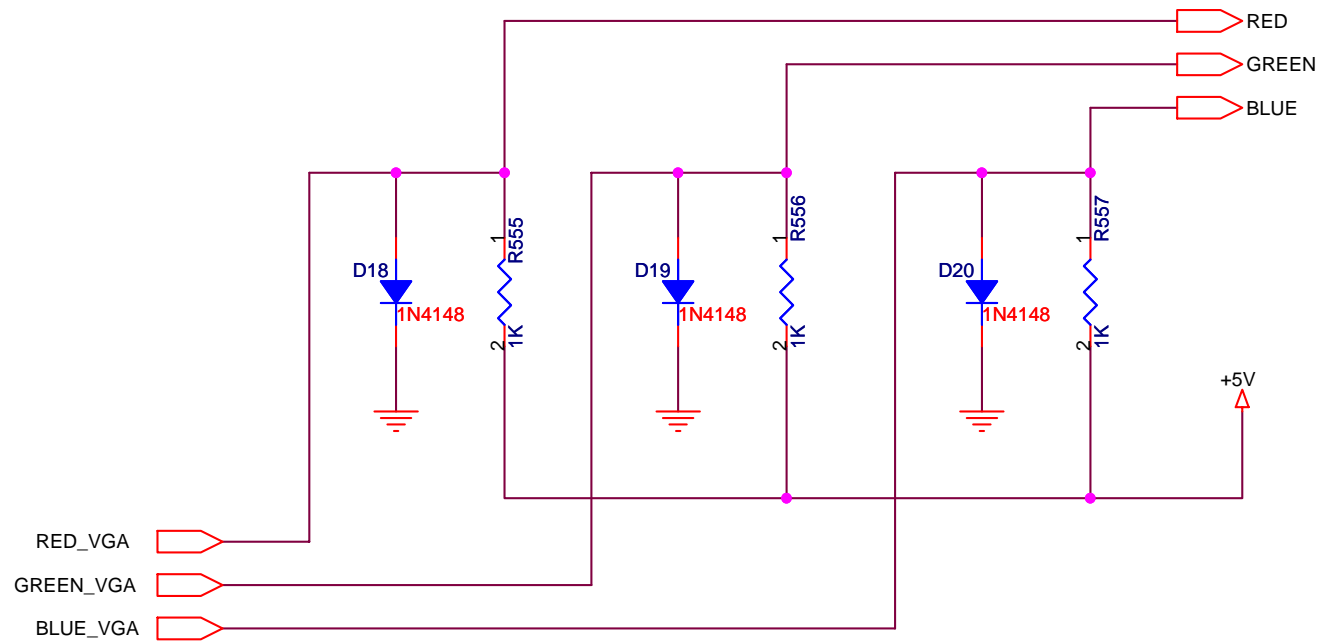
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SER2



## SERIAL PORT (FULL MODEM)

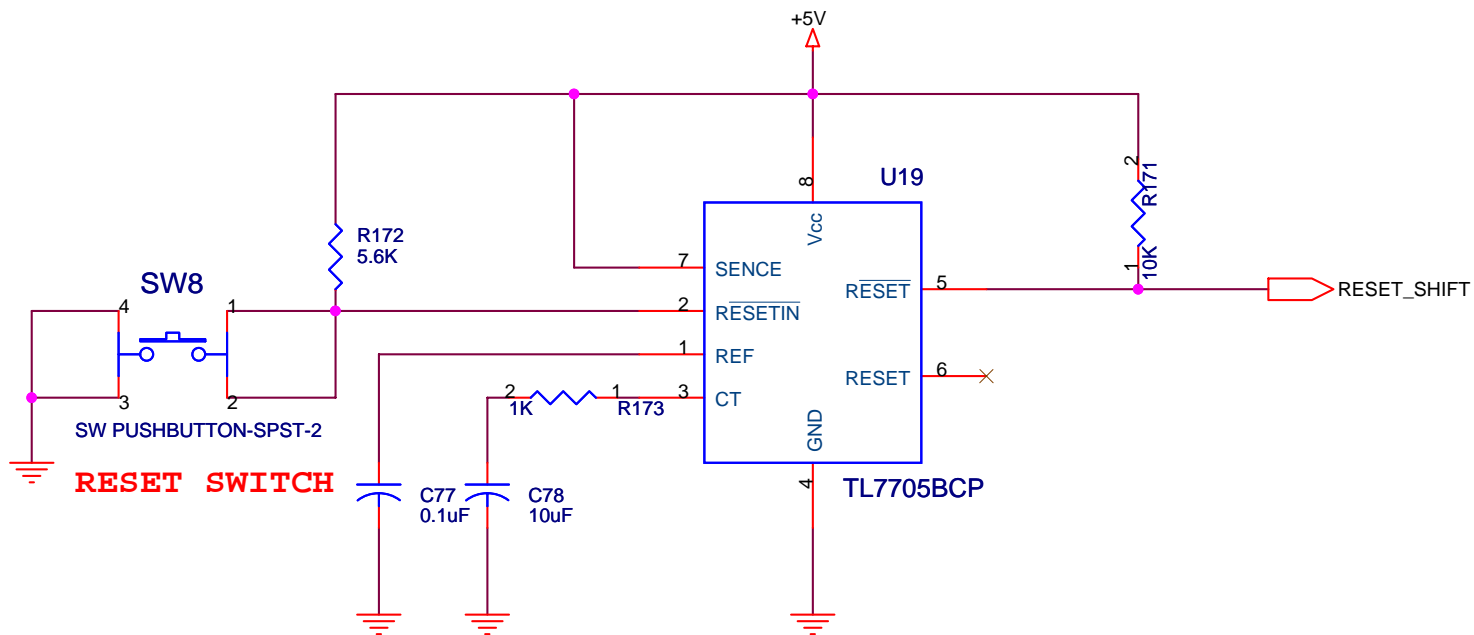
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## VGA INTERFACE

NOTE: LEVEL SHIFTING, SEE PAGE3\_PPT

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**NOTES:**

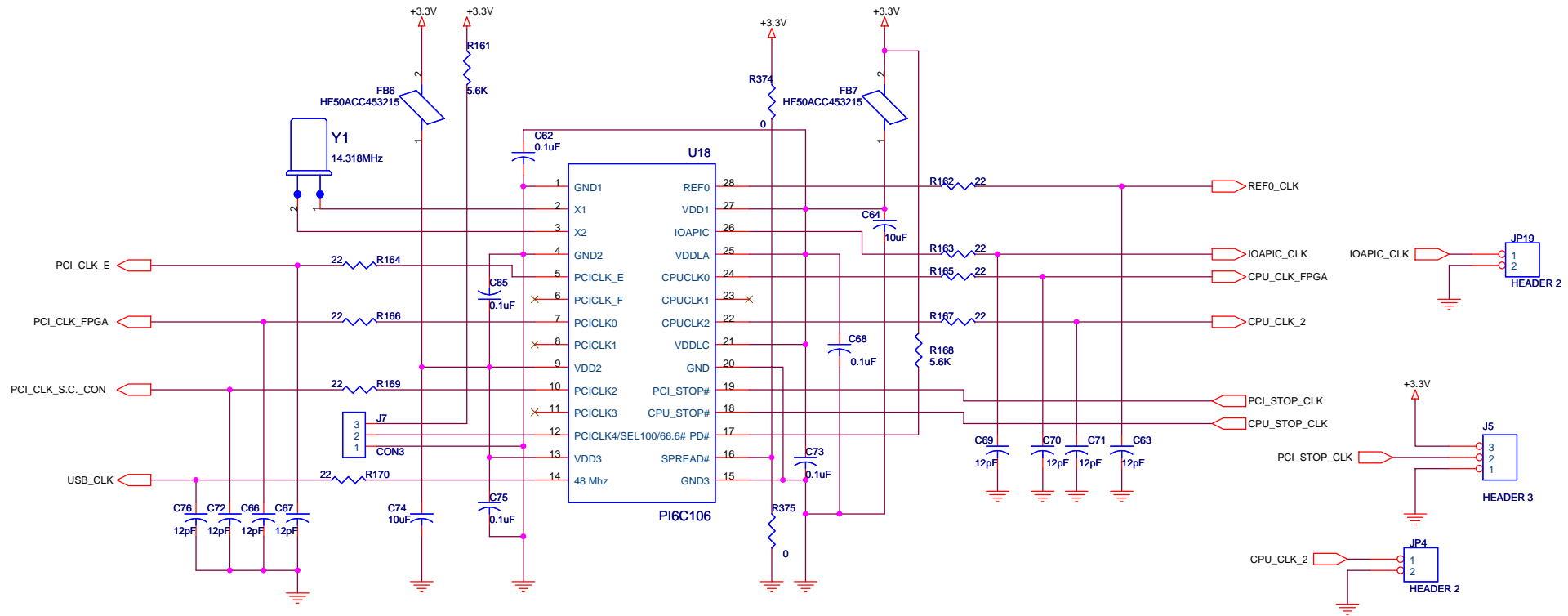
[1] RESET TIME  $T_d = 2.6 \times 10E4 (C_t)$

[2] FOR LEVEL SHIFTING, SEE PAGE 9 LCD\_DISPLAY.

**RESET CIRCUIT**

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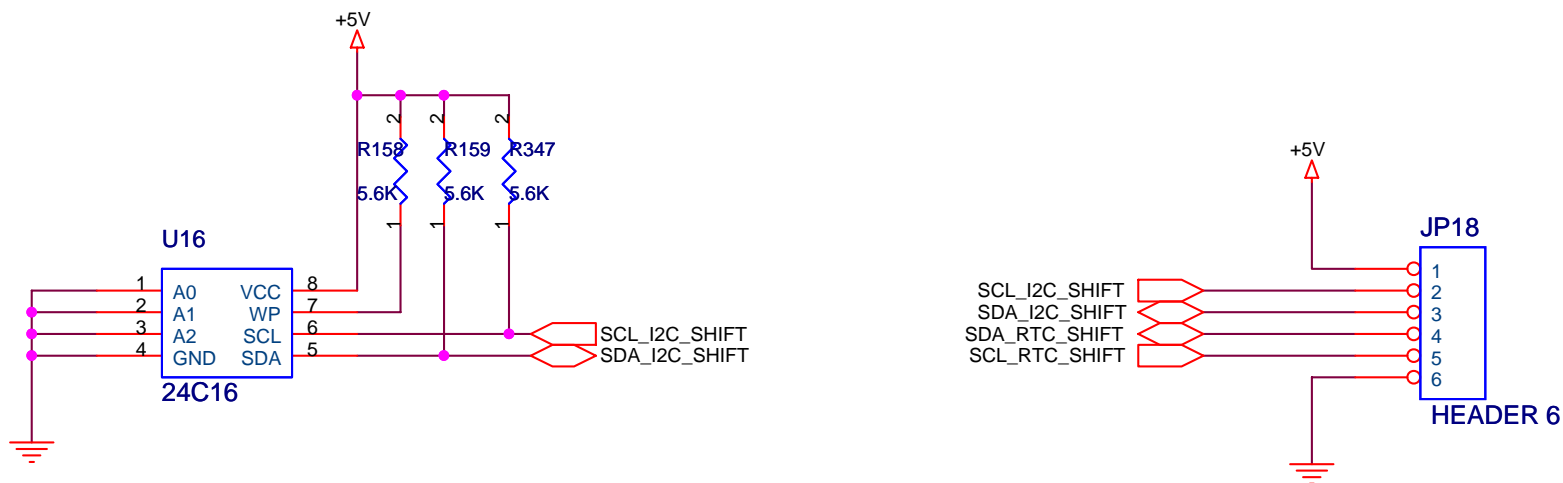
**NOTES:**

- [1] CONNECTOR PROVIDE HIGH OR LOW LEVEL ACCORDING TO GET 100Mhz / 66.6Mhz
- [2] 12pF CAPACITORS ARE USED AS EMI REDUCING CAPACITORS
- [3] HERE WE PROVIDE STUFFING OPTION FOR SPREAD INPUT

STUFFED R374 - DEFAULT HIGH  
STUFFED R374 - ENABLE SPREAD#

**MASTER CLOCK GENERATOR**

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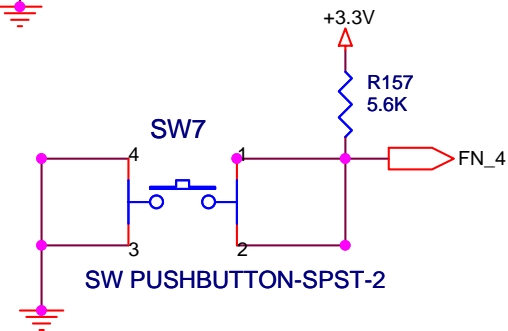
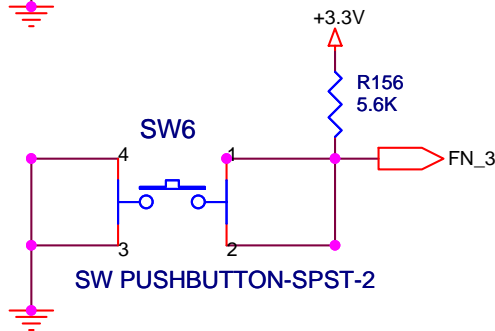
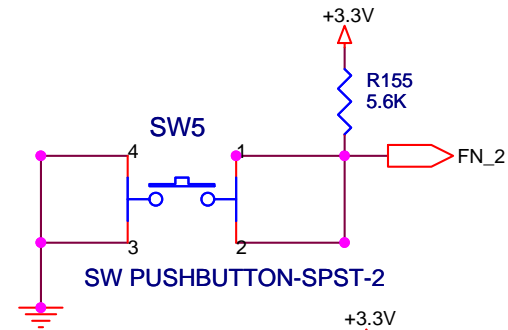
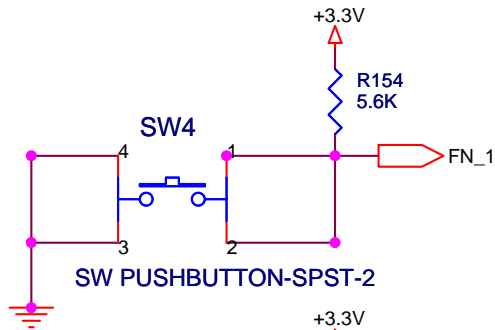
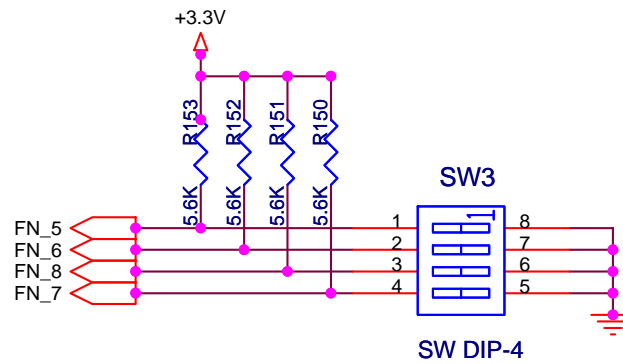


**NOTE:**

- [1] R158 IS NOT STUFFED (WP PIN IS KEPT FLOATING) FOR NORMAL OPERATIONS  
- STUFF R158 TO ENABLE WRITE PROTECTOIN IN THE SUPPOTED DEVICE
- [2] FOR LEVEL SHIFTING, SEE PAGE\_10\_L.S. (FOR S.C. CONN.)

**I2C\_PROM**

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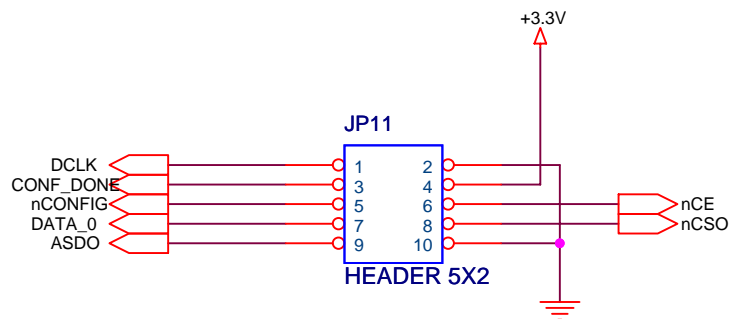
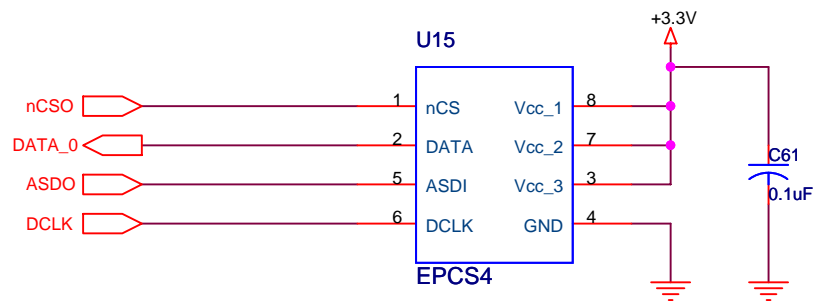


#### NOTES:

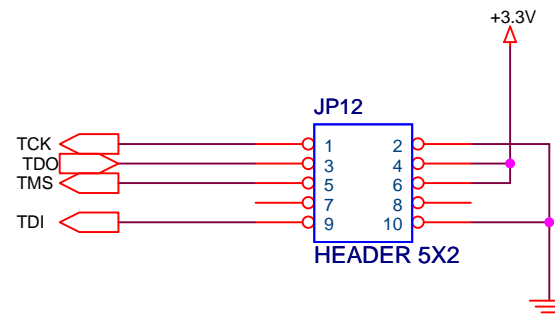
- [1] HERE FOUR USER DEFINABLE PUSH BUTTON SWITCHES ARE SHOWN
- [2] THE PUSH BUTTON SWITCH FOR SYSTEM RESET IS SEPARATELY DEFINED ON PAGE 16 (RESET CIRCUIT)
- [3] BE CAREFUL WHEN MOUNTING THE DIP SWITCH

## PUSH BUTTONS & DIP SWITCHES

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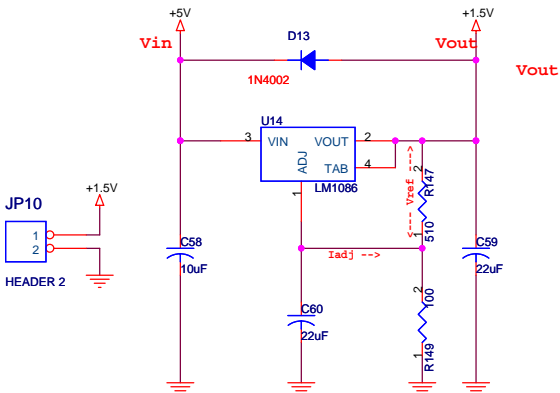
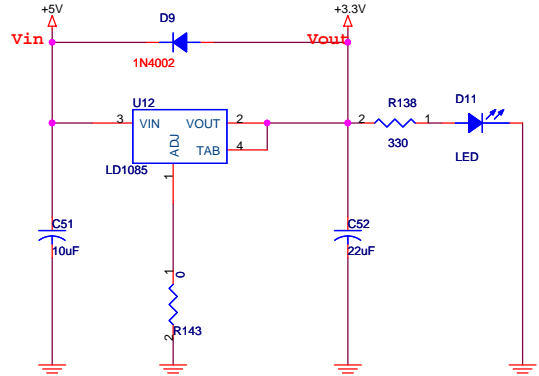
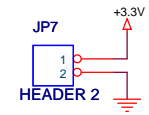
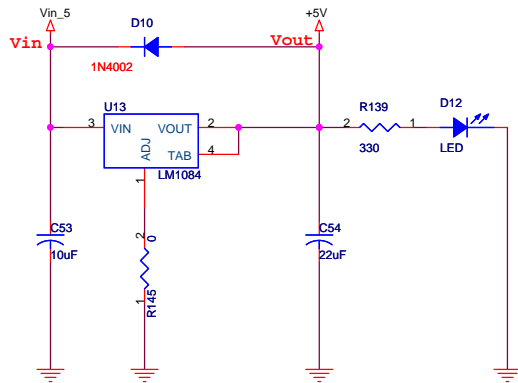
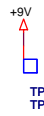
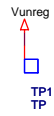
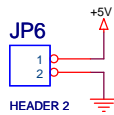
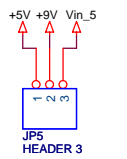
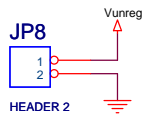
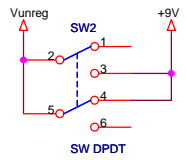
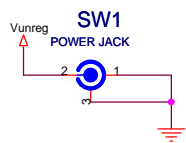
BYTE BLASTER II 10 PIN MALE HEADER  
AS MODE [DCLK(FPGA) => DCLK(CONFIG. PROM)]



BYTE BLASTER II 10 PIN MALE HEADER  
JTAG CONFIGURATION

## CONFIGURATION PROM

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Vref = 1.25V  
Iadj = 50uA

## POWER SUPPLY CIRCUIT

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396  
TP

397  
TP

398  
TP

399  
TP

Stand Off pts.

441  
TP

442  
TP

443  
TP

444  
TP

Crop pts.

447  
TP

448  
TP

449  
TP

Moire pts.

402  
TP

403  
TP

445  
TP

446  
TP

Fiducial Points

405  
TP

406  
TP

407  
TP

408  
TP

409  
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410  
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411  
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412  
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413  
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TP

HEAT SINK POINTS

Mfg. Points

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