
This file lists pin difference between UP3 -1C6 and UP3 – 1C12 boards.

For the most up to date information please visit

<http://www.slscorp.com/UP3Support/pages/documents.php>

The following Table describes the Pin difference between the UP3-1C6 and UP3-1C12 versions:

Sr. No.	FPGA Pin	EP1C6 Version		EP1C12 Version	
		Port Name	Affected Port	Port Name	Affected Port
1	80	RY/BY_FL	U8.15	GND	-
2	81	AD_18_FL	U8.16	VCCINT	-
3	96	DQ_01_SR_SD_FL_LCD	U8.31, U6.4, U7.8, U1.8	GND	-
4	97	DQ_09_SR_SD_FL	U8.32, U6.44, U7.30	VCCINT	-
5	102	DQ_04_SR_SD_FL_LCD	U8.38, U6.8, U7.13, U1.11	GND	-
6	103	DQ_12_SR_SD_FL	U8.39, U6.48, U7.35	VCCINT	-
7	198	IO_42_FPGA	J2.14	VCCINT	-
8	199	IO_51_FPGA	J3.21	GND	-
9	204	IO_56_FPGA	J3.31	VCCINT	-
10	205	IO_57_FPGA	J3.29	GND	-
11	220	IO_61_FPGA	J3.4	VCCINT	-
12	221	IO_64_FPGA	J3.10	GND	-
13	126	IO_01_FPGA	J1.37	RY/BY_FL	U8.15
14	125	IO_00_FPGA	J1.38	AD_18_FL	U8.16
15	133	IO_05_FPGA	J1.33	DQ_01_SR_SD_FL_LCD	U8.31, U6.4, U7.8, U1.8
16	132	IO_04_FPGA	J1.34	DQ_09_SR_SD_FL	U8.32, U6.44, U7.30
17	128	IO_03_FPGA	J1.35	DQ_04_SR_SD_FL_LCD	U8.38, U6.8, U7.13, U1.11
18	127	IO_02_FPGA	J1.36	DQ_12_SR_SD_FL	U8.39, U6.48, U7.35
19	181	IO_29_FPGA	J1.24	IO_42_FPGA	J2.14
20	180	IO_28_FPGA	J1.23	IO_51_FPGA	J3.21
21	177	IO_31_FPGA	J1.26	IO_56_FPGA	J3.31
22	175	IO_30_FPGA	J1.25	IO_57_FPGA	J3.29
23	169	IO_27_FPGA	J1.22	IO_61_FPGA	J3.4
24	168	IO_26_FPGA	J1.21	IO_64_FPGA	J3.10

Notes:

- FL indicates FLASH Memory
- SR indicates SRAM Memory
- SD indicates SDRAM Memory
- All the prefixes (e.g., RY/BY, AD_18, DQ_09, etc.) indicate corresponding port connectivity on the related devices
- All the IO_xx_FPGA are wired to the Santa Cruz Headers as mentioned in the above table

Important Note:

- The EP1C6 device on the UP3-1C6 board has 185 IOs, where as the EP1C12 device on the UP3-1C12 board has 173 IOs, hence 12 less IOs are available in the UP3-1C12 version compared to the UP3-1C6 board, i.e., the Santa Cruz header connections shown in the above table for UP3-1C6 (Sr. No. #13 to #24) are not available in the UP3-1C12 Version
- EP1C12 pin changes affect the shared Memory Sub-System and the Santa Cruz Connector only, everything else remains the same

The following table helps easy translation of the EP1C6 based designs to the EP1C12 based designs:

Sr. No.	Port Name	Affected Port	FPGA Pin	
			EP1C6 Version	EP1C12 Version
1	RY/BY_FL	U8.15	80	126
2	AD_18_FL	U8.16	81	125
3	DQ_01_SR_SD_FL_LCD	U8.31, U6.4, U7.8, U1.8	96	133
4	DQ_09_SR_SD_FL	U8.32, U6.44, U7.30	97	132
5	DQ_04_SR_SD_FL_LCD	U8.38, U6.8, U7.13, U1.11	102	128
6	DQ_12_SR_SD_FL	U8.39, U6.48, U7.35	103	127
7	IO_42_FPGA	J2.14	198	181
8	IO_51_FPGA	J3.21	199	180
9	IO_56_FPGA	J3.31	204	177
10	IO_57_FPGA	J3.29	205	175
11	IO_61_FPGA	J3.4	220	169
12	IO_64_FPGA	J3.10	221	168
13	IO_01_FPGA	J1.37	126	NA
14	IO_00_FPGA	J1.38	125	NA
15	IO_05_FPGA	J1.33	133	NA
16	IO_04_FPGA	J1.34	132	NA
17	IO_03_FPGA	J1.35	128	NA
18	IO_02_FPGA	J1.36	127	NA
19	IO_29_FPGA	J1.24	181	NA
20	IO_28_FPGA	J1.23	180	NA
21	IO_31_FPGA	J1.26	177	NA
22	IO_30_FPGA	J1.25	175	NA
23	IO_27_FPGA	J1.22	169	NA
24	IO_26_FPGA	J1.21	168	NA