
This file errata.txt lists updates for the UP3 Reference Manual.

For the most up to date information please visit

<http://www.slscorp.com/UP3Support/pages/tutorial.php>

Updates for the UP3 - 1C6 Reference Manual:

UP3 - 1C6 Reference Manual has two revisions.

- UP3- 1C6 Reference Manual Version 1.0.0
- UP3- 1C6 Reference Manual Version 1.0.2

List of the changes made in UP3- 1C6 Reference Manual version 1.0.2

1. **Table 13:IDE** FPGA Pin number for **DMACK** and **A0** (IDE Pins) has been corrected for IDE in P3- 1C6 Reference Manual Version 1.0.2,(Page 36).
2. **Usage of I2C Memory** have been corrected in UP3 - 1C6 Reference Manual version 1.0.2.
 - Usage of I2C memory in UP3 - 1C6 Reference Manual version 1.0.0 (Page 40).
 - It can be tied HIGH with 5.6Kohm resistor to write protect the upper half of the memory.
 - Usage of I2C memory in UP3 - 1C6 Reference Manual version 1.0.2 (Page 40).
 - The Write Protect (WP) pin can be tied HIGH with 5.6K resistor to write protect the entire memory.
3. **Table 17: Headers for I2C Bus** has been corrected (Page 41).
 - Table 17: Header for I2C Bus in UP3 - 1C6 Reference Manual version 1.0.0

JP18 Pin No.	Signal Description
1	GND
2	SCL - I2C Bus on which RTC is connected
3	SDA - I2C Bus on which RTC is connected
4	SDA - I2C Bus on which PROM is connected
5	SCL - I2C Bus on which PROM is connected
6	VCC +5 Volt

- Table 17: Header for I2C Bus in UP3 - 1C6 Reference Manual version 1.0.2

JP18 Pin No.	Signal Description
1	VCC +5 Volt
2	SCL - I2C Bus on which I2C EEPROM is connected
3	SDA - I2C Bus on which I2C EEPROM is connected
4	SDA - I2C Bus on which I2C RTC is connected
5	SCL - I2C Bus on which I2C RTC is connected
6	GND

4. **LED Configuration Description** has been corrected (page 51).

- LED Configuration Description in UP3 - 1C6 Reference Manual version 1.0.0
 - All of them are active low driven (Common Anode). The LED will glow when there is logic '0' at FPGA pin.
- LED Configuration Description in UP3 - 1C6 Reference Manual version 1.0.2
 - All of them are active high driven (Common Cathode configuration). All the LEDs will glow when there is logic '1' at the corresponding FPGA pins.

5. **Table-27 Clocking Chip Pin Configuration** of UP3- 1C6 Reference Manual Version 1.0.0(page 54) has been moved to Appendix of UP3- 1C6 Reference Manual Version 1.0.2(page 56)

6. **Table 29 : Jumper Setting for Clock Input** to the FPGA at CLK3 has been corrected (Page 55).

- Table 29: Jumper Setting for Clock Input to FPGA at CLK3 in UP3 - 1C6 Reference Manual version 1.0.0S

CLK3	Jumper Setting	FPGA Pin No
PCICLK_E (U18.5)3.33MHz	Short JP3.8 & JP3.7	152
REF0CLK (U18.28) 4.318 MHz	Short JP3.8 & JP3.6	152

- Table 28: Jumper Setting for Clock Input to FPGA at CLK3 in UP3 - 1C6 Reference Manual version 1.0.2

CLK3	Jumper Setting	FPGA Pin No
PCICLK_E (U18.5)33.33MHz	Short JP3.8 & JP3.7	152
REF0CLK(U18.28)14.318 MHz	Short JP3.8 & JP3.6	152

7. **Table 30: CPU Clock Select Setting** has been corrected (Page 55).

- Table 30: CPU Clock Select Setting in UP3 - 1C6 Reference Manual version 1.0.0

CLK3	Jumper Setting	FPGA Pin No
66 MHz	Short JP 7.1 & JP 7.2	153
100 MHz	Short JP 7.2 & JP 7.3	153

- Table 29: CPU Clock Select Setting in UP3 - 1C6 Reference Manual version 1.0.2

CLK3	Jumper Setting	FPGA Pin No
66 MHz	Short J 7.1 & J 7.2	153
100 MHz	Short J 7.2 & J 7.3	153

8. **Table 33: Reset Signal Assignment** has been modified to remove RESET Chip related information from the table (Page 57).

- Table 33: Reset Signal Assignment in UP3 - 1C6 Reference Manual version 1.0.0

U19 Reset IC Pin No.	Signal	FPGA Pin No.	Connection
1	REF	-	-
2	RESETIN#	-	SW8
3	CT	-	-
4	GND	-	-
5	RESET#	23	-
6	RESET	-	NC
7	SENCE +5 V	-	-
8	VCC +5V	-	-

- Table 32: Reset Signal Assignment in UP3 - 1C6 Reference Manual version 1.0.2

U19 Reset IC Pin No.	Signal	FPGA Pin No.	Connection
2	RESETIN#	-	SW8
5	RESET#	23	-