Schematic D-Flip Flop

Tutorial One

Version 1.0

UP3 Education Kit

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Introduction

This tutorial will guide one through the basic features of the Quartus II software. It explains how to design, compile, simulate and program your logic designs in the Quartus II software using a D-Flop.

A design using a D-Flop will be created and assigned FPGA pins according to the UP3 board layout. In this particular case, the D input will be controlled by a DIP switch, the CLK input will be controlled by a Push-Button Switch. The output Q shall be assigned to an LED so that the functionality may be visually observed.

Start Lesson

Section 1: Project Creation

The Quartus II software offers a New Project wizard to help create a new project. The project settings may be changed using menu commands and dialog boxes. To create a new project using the New Project Wizard, follow the steps below:

1. Choose **New Project Wizard** (File menu). The New Project Wizard appears as shown in Figure 1. Opening the New Project Wizard for the first time may display the Introduction page; click Next to proceed to the first page of the wizard.

   Click on the check box **"Don't show..."** to disable the dialog box from appearing the next time the wizard is run.

FIGURE 1. New Project Wizard

In either case, click **Next**

A new dialog box, as shown in Figure 2, appears asking for working directory and related information.

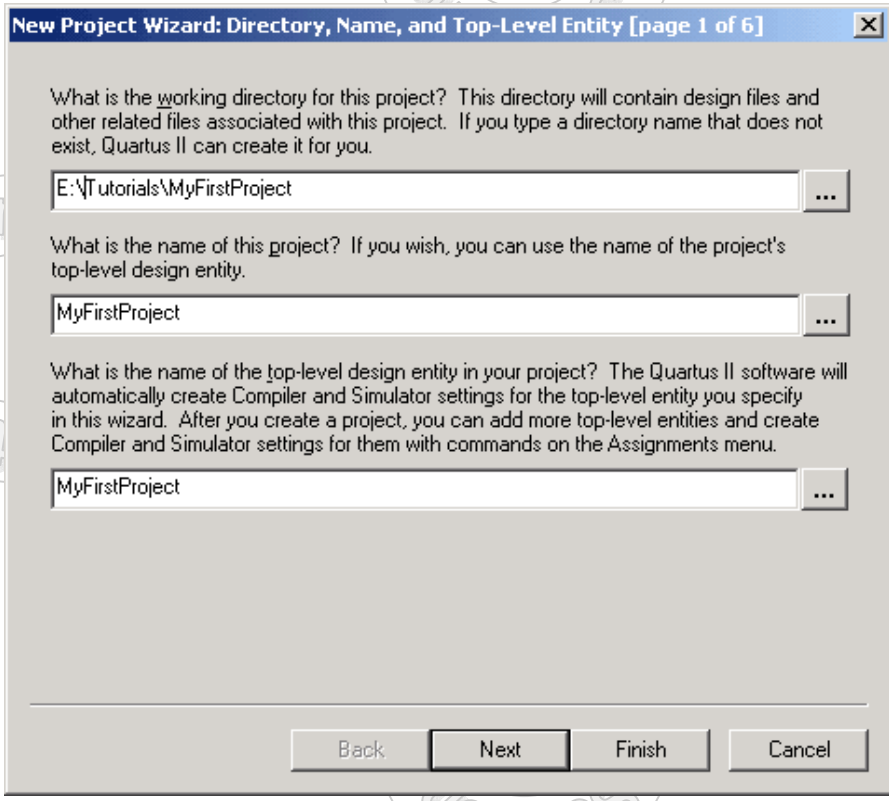
2. Type the directory name in the working directory box, or select the directory with **Browse** (...).

It is a good idea to create a new directory to encapsulate the design. So within the Tutorial directory create a new directory called **MyFirst-Project**. (Click on the folder with a star).

3. Type a name for the project in the project name box. If not automatically entered for by the tool, then for this example, type **MyFirstProject**.
4. Type **MyFirstProject** as the name of the top-level design entity of the project in the top-level design entity box.

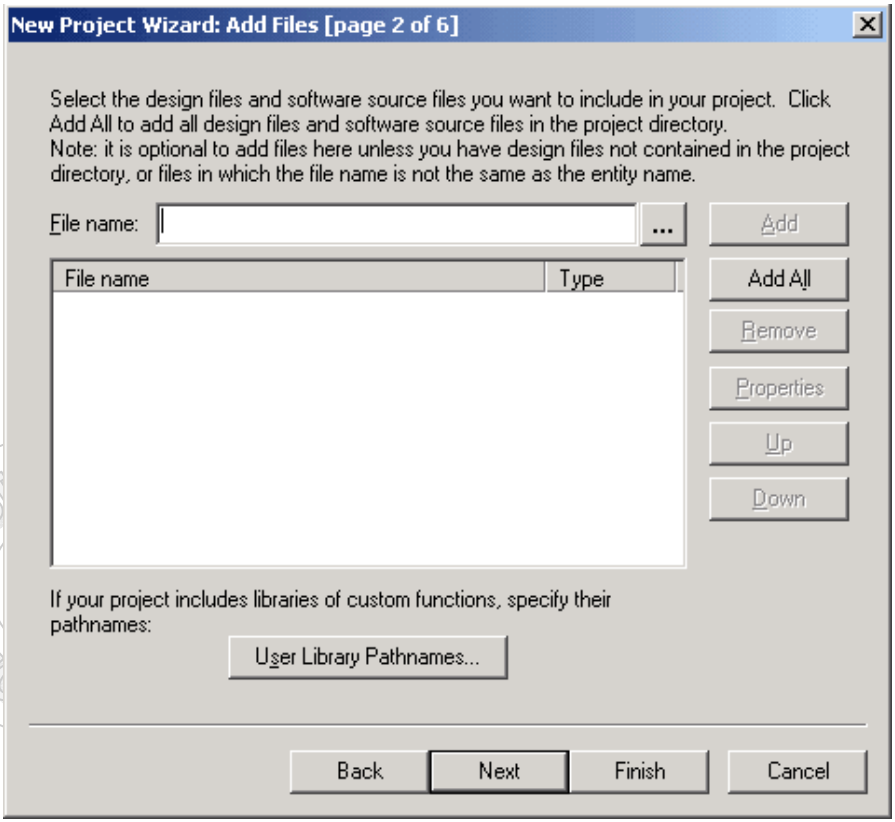
   This must be the exact name of the top-level module.
5. Click **Next**

FIGURE 2. Top Level Entry



6. The **Add Files** page appears as shown in Figure 3. In this particular case, no design files pre-exist. However if the design files already existed for the project, simply click on **Browse** (...) to select the appropriate files, and then click **Add** to add them to the project.

FIGURE 3. Add Files

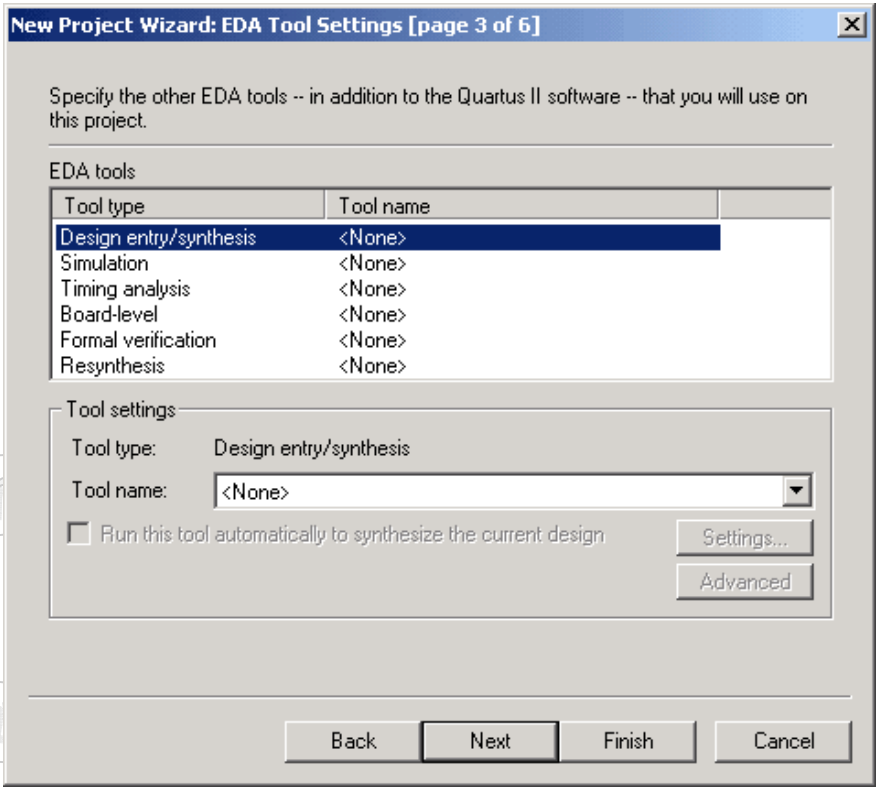


7. Click **Next**

The **EDA Tool Settings** page dialog, as shown in Figure 4, appears. This page allows one to specify options for other EDA tools for use

with this project. Since this project does not use any other EDA tools, make sure that **None** is specified in the **Tool name** column for each tool type.

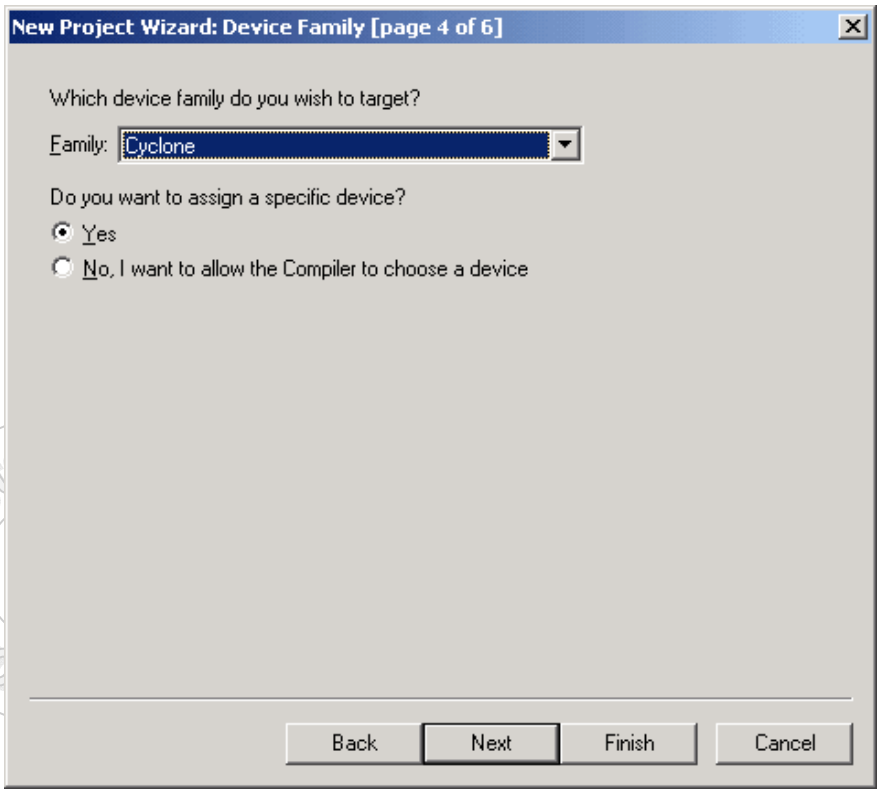
FIGURE 4. EDA Tool Setting



Click **Next**

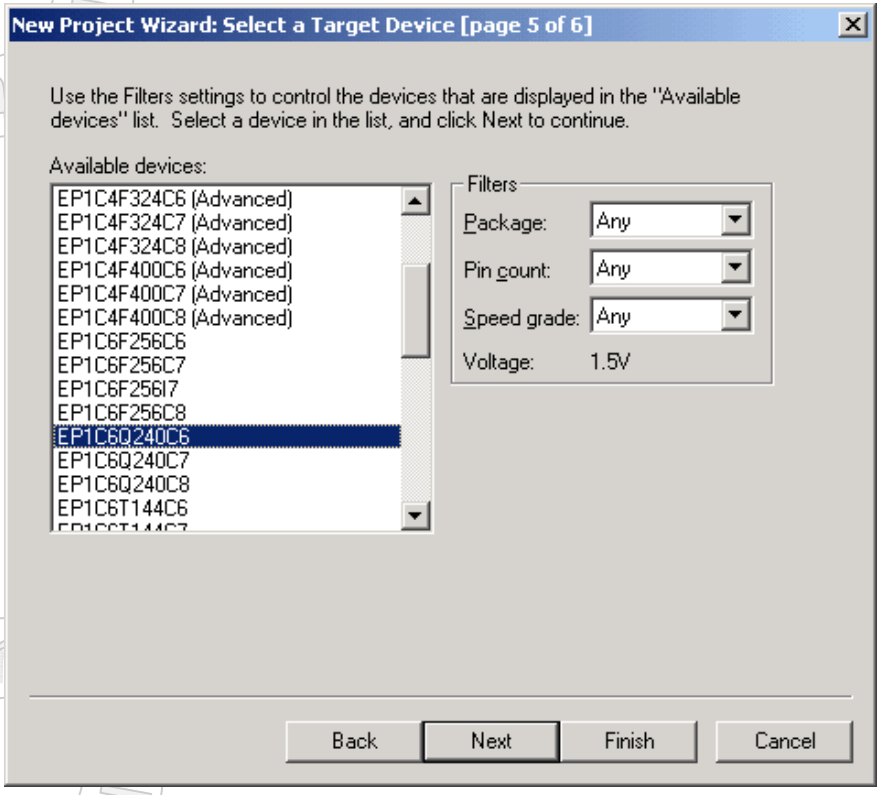
8. The next dialog box, as shown in Figure 5, asks for specific information related to the hardware. Select the target family. Since the board uses a **Cyclone** device, select the Cyclone family. Then select the **YES** button, to target a specific device, namely the **EP1C6Q240C8** on the shown in Figure 6.

FIGURE 5. Device Family



9. Click **Next**.
10. Scoll down the list or use the package, pin or speed grade drop down boxes to select the part. Again, select **EP1C6Q240C8**.

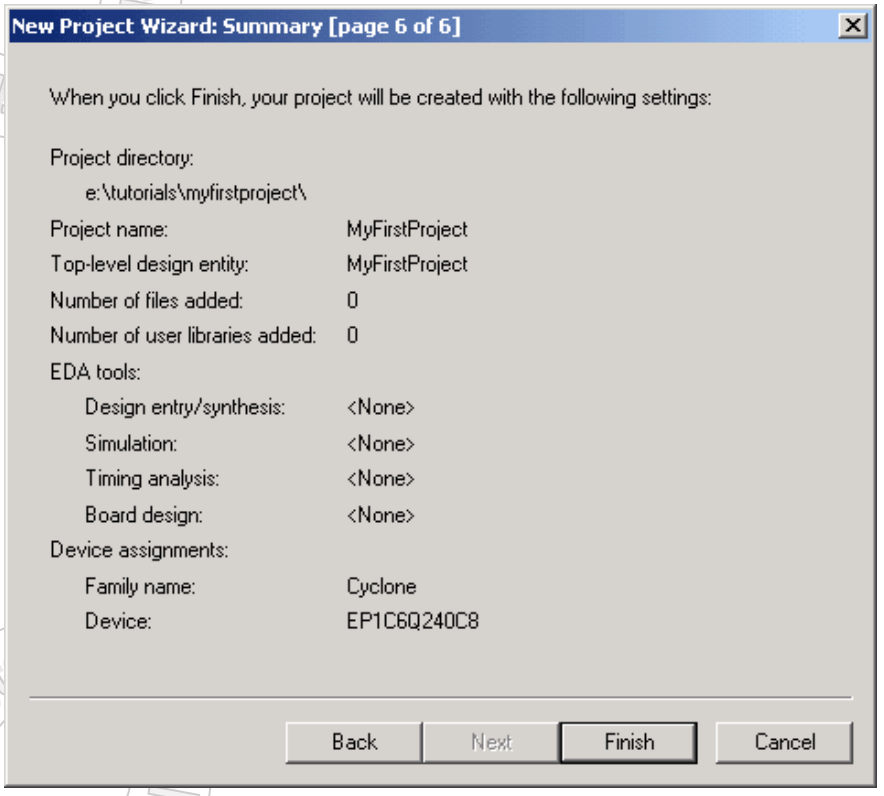
FIGURE 6. Target Device



11. Click **Next**

The last dialog box, as show in Figure 7, displays the **Summary** for the entire project.

FIGURE 7. Project Summary

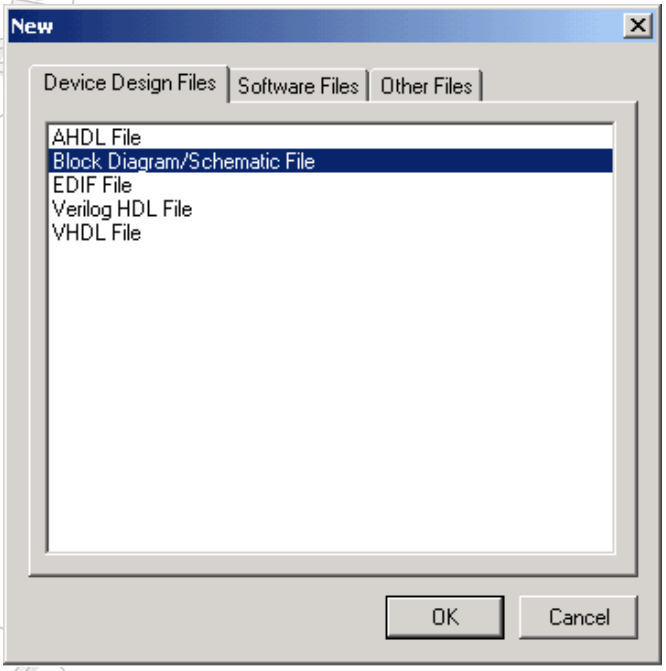


Section 2: Schematic Entry

After creating the project, the design must be entered. Quartus II allows a number of methods of design entry. Completion of the following steps will show how to create a schematic and include it in the project. The objective is to instantiate a D-flop and assign it to the proper pins.

1. First create new file by **File -> New** … or simply clicking on the new file icon.
2. As Figure 8 shows below, select **Block Diagram/Schematic** File then click **OK**

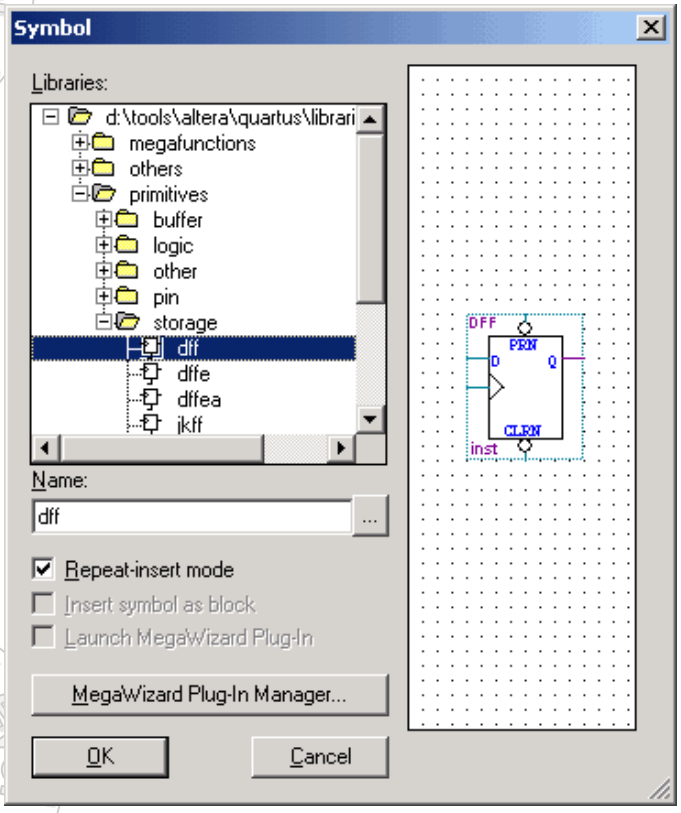
FIGURE 8. New File



A temporary file with the name Block1.bdf is created. Notice the grid and side toolbar.

3. Using the side toolbar, click on the **"and gate" like icon**. This is the symbol tool.
4. Figure 9 shows the dialog box that pops up. Under the libraries category click on the **"+"** to expand the category and choose the symbol required. In this case it is storage primitive dff. Then click on **OK**.

FIGURE 9. Symbol Insertion

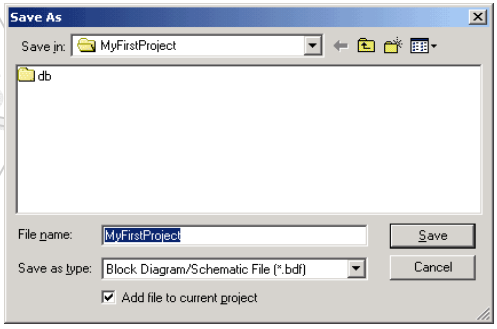


5. Now the symbol will show up in the main schematic window so simply move the symbol to the desired location and **left click.**
6. After placing one instance, click on the "arrow" icon in the vertical toolbar or press **ESC**.
7. Repeat Step 4.
8. This time choose primitive pin **input**. Click **OK**.

9. Place two instances of the input--one for the D input and the other for the Clk(shown as a greater than sign). Make sure that the newly placed instances touch the dff inputs. If not the input primitives may be connected using the Orthogonal Node Tool found on the left vertical tool bar.
10. Repeat Step 4
11. Choose primitive pin **output**. Click **OK**.
12. Place the output pin instance on Q. Then press **ESC**.
13. To zoom in or out use the Zoom Tool.
14. Before proceeding, it is a good idea to save the diagram.

    File -> Save … or simply clicking on the save file icon.
15. Below, Figure 10 shows the dialog box. Make sure that **"Add file to current project"** is checked. The file name field is pre-filled with MyFirstProject which is the name of the entire project. Keep this name as the default. Click **Save**. As an exercise after completion of this tutorial, use a different name and observe what happens.

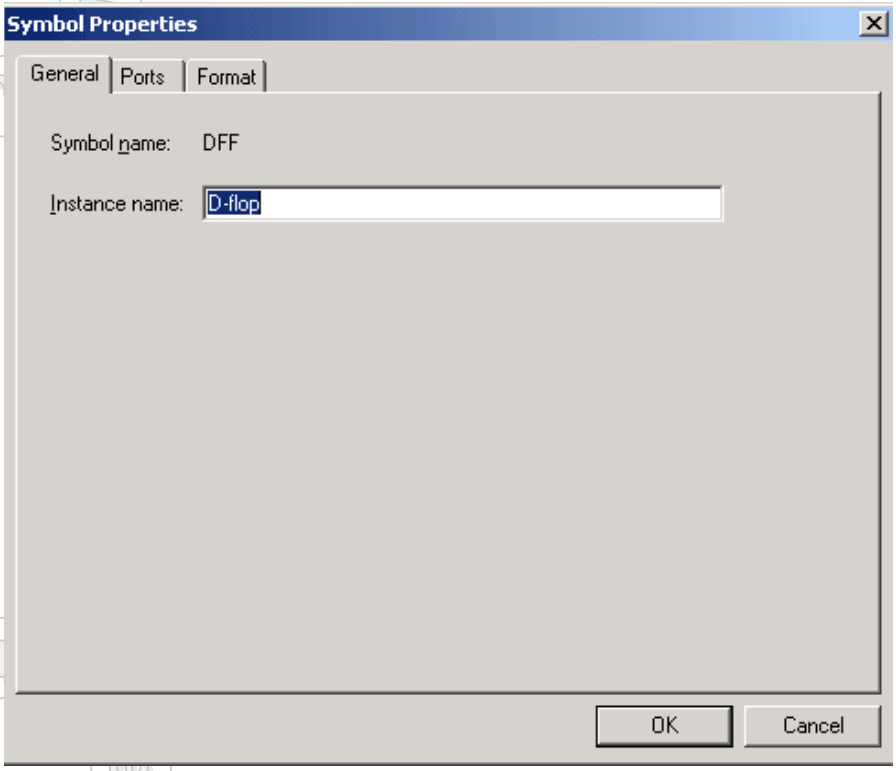
FIGURE 10. Save Dialog



16. The instantiated primitives need unique names. Double Click on the **DFF primitive** after which the following dialog box appears (Figure 11). Change the instance name field to **DFlop** and Click **OK**

    Another way is to double click on the instance name directly and change it there.

FIGURE 11. Symbol Properties



17. Repeat step 17 for the input primitives with the following names: **DIn** and **ClkIn**.
18. Repeat step 17 for the output primitives with the following name: **QOut**.

Now for the most important part-the assignment of the design pins to the physical FPGA pin location. In the board reference manual please refer to the sections on Push Button Switches, DIP Switches,

and LEDs. The named pins must be assigned as specified in the table below.

TABLE 1. Board Connectivity

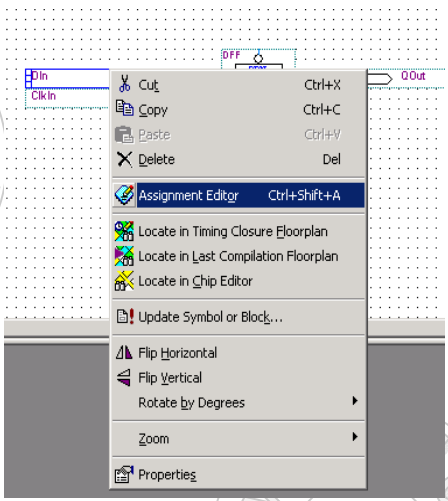
Design Pin Name	FPGA Assignment	Board Function
DIn	Pin 58	DIP Switch-SW3.1
ClkIn	Pin 48	Push Button-SW4
QOut	Pin 56	LED-D3

Confirm the above by looking at the reference manual.

The pin assignment editor may be invoked in multiple ways.

19. As an example, **Right Click on DIn** and select **Assignment Editor**. Figure 12 shows the invoked dialog box.

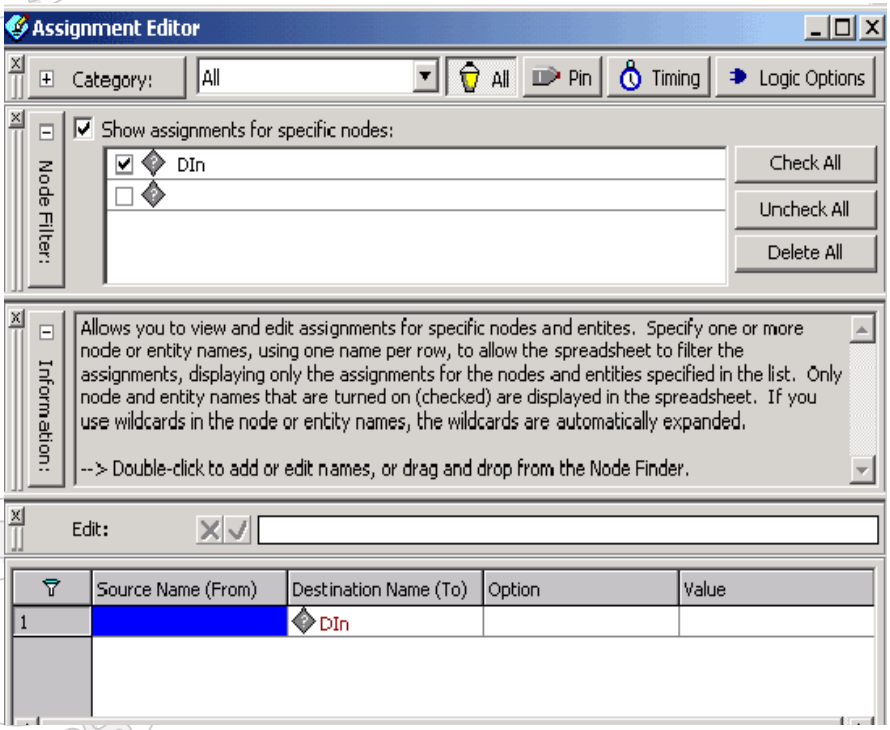
FIGURE 12. Pin Assignment



Another way is to select the DIn input pin and enter **Ctrl+Shift+A**. And yet another way is to select the DIn input pin and then from the

menu bar **Assignments -> Assignment Editor**. Figure 13 below shows the dialog box.

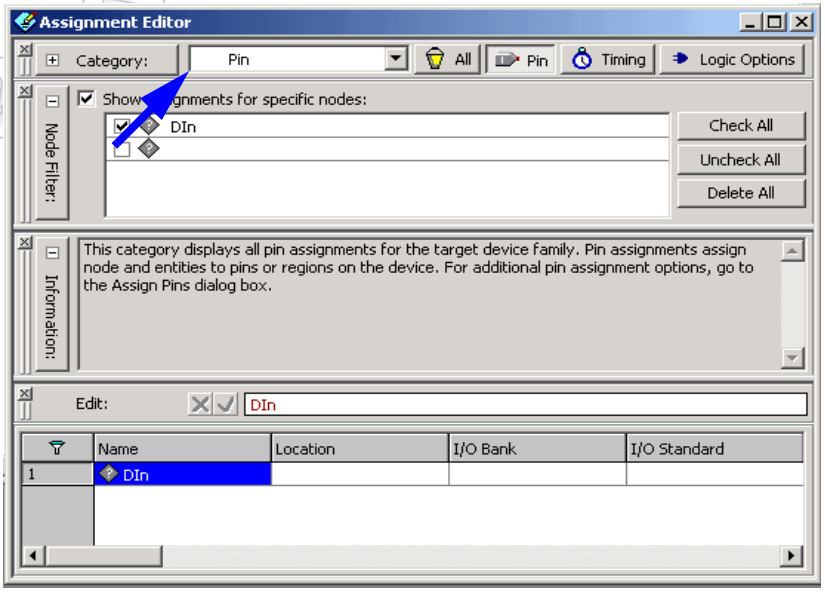
FIGURE 13. Assignment Editor



This is a very busy window. There are many things that can be done with it. But since the intention is to assign a FPGA pin number to DIn, follow the steps below.

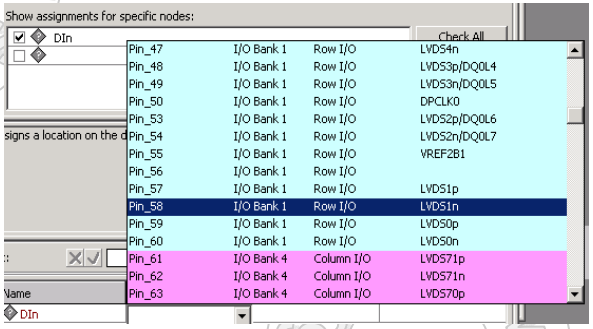
20. Under Category, Click on **Pin**. The editor should look like the Figure 14 below.

FIGURE 14. Assigning the Pins



21. In the Edit section, Double Click on **Location** and a drop down menu like Figure 15 appears. Select Pin_58 for DIn.

FIGURE 15. Pin Location



22. Then Click on **Name** for the Editor to accept the selection
23. **Close** the assignment editor window.

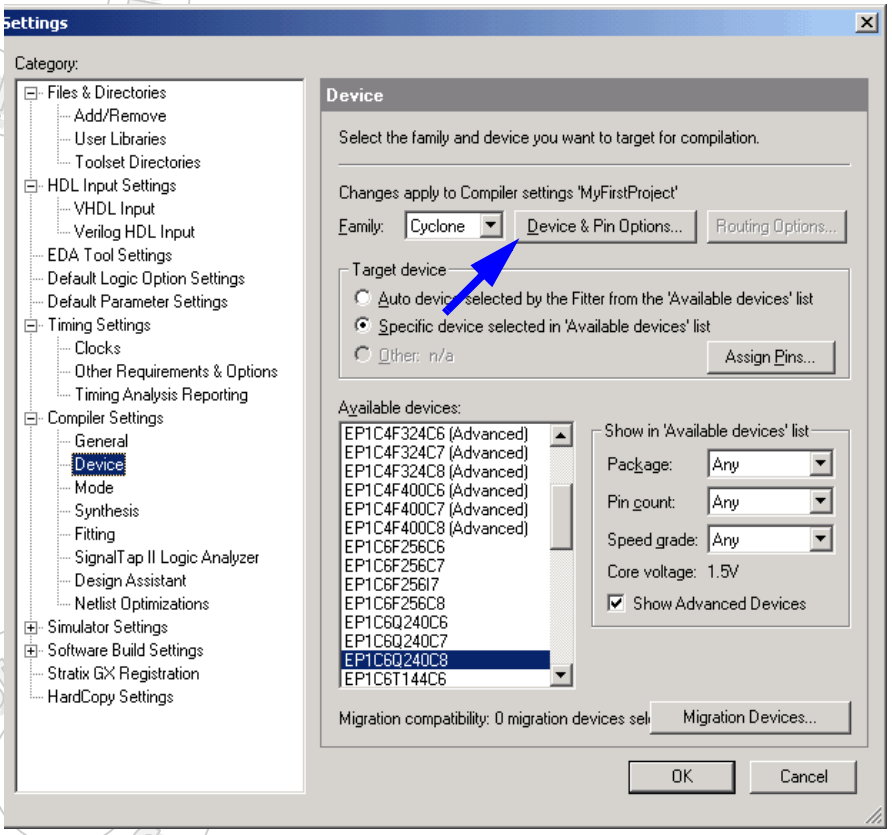
24. A message will pop asking to save. Click **Yes**
25. Another message stating messages generated during save pops up. Click **OK**
26. **Repeat** Steps 20 thru 26 for the rest of the pins.

Section 3: Compilation

The Quartus II software allows compilation of an entire design, or any constituent part of a design. The "compilation focus," which is the design entity needing compilation, may be selected from any portion of the project hierarchy.

1. Before actually compiling the design, one should set the appropriate Compiler settings by pressing **Ctrl+Shift+E** or on the menu bar **Assignments -> Settings**. Please see Figure 16. Three major compiler settings are required and explained in the steps below.
   - Generate a Compressed Bit Stream.
   - Set Configuration Scheme to Active Serial and use Configuration Device EPCS1
   - Since the Cyclone device on the board connects to many other ICs and Connectors, one should set the unused pins as tri-stated inputs. This will tri-state the unused FPGA pins such that it doesn't drive other logic and potentially causing large currents to flow.

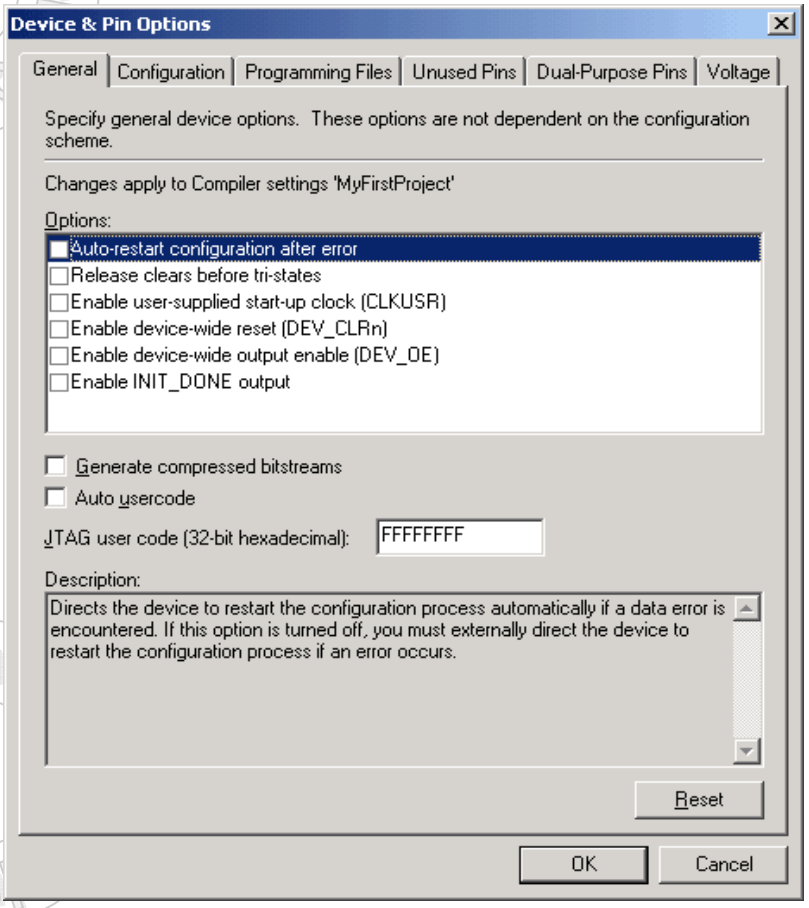
FIGURE 16. Compiler Settings



1. Next to the Family category, Click on **Device and Pin Options**

Now a new window will pop up allowing changes for some advanced configuration operations. Figure 17 shows the dialog.

FIGURE 17. Device and Pin Options



2. Under the **General Tab**, click on the Generate compressed bit-streams check box.
3. Under the **Configuration Tab**, set the configuration scheme to **Active Serial**
4. Under the **Configuration Tab**, set the configuration device to **EPCS1**
5. Under the **Unused Pins**, select radio button **As inputs, tristated**

6. After completion of the above steps click **OK** to close the Device & Pin options diaglog
7. Then click **OK** to close the Settings dialog

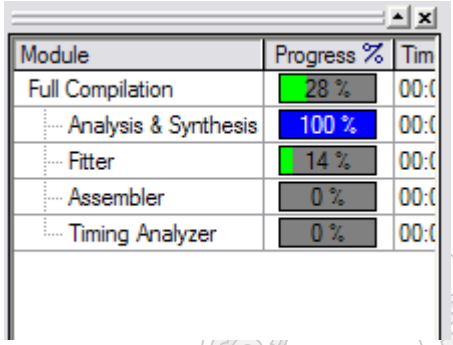
Now the design is ready for acutal compiliation. Again, there are several access mechanisms to perform the compile option.

- Use the standard quartus II tool bar and click on the Start Compliation icon
- On the menu bar under Processing click on Start Compilation
- Press Crtl-L

8. For this tutorial **Press Ctrl+L**

The complier will start and the left side of Quartus should show the status. Full compilation consists of Analysis and Synthesis, Fitting, Assembling and Timing Analysis.

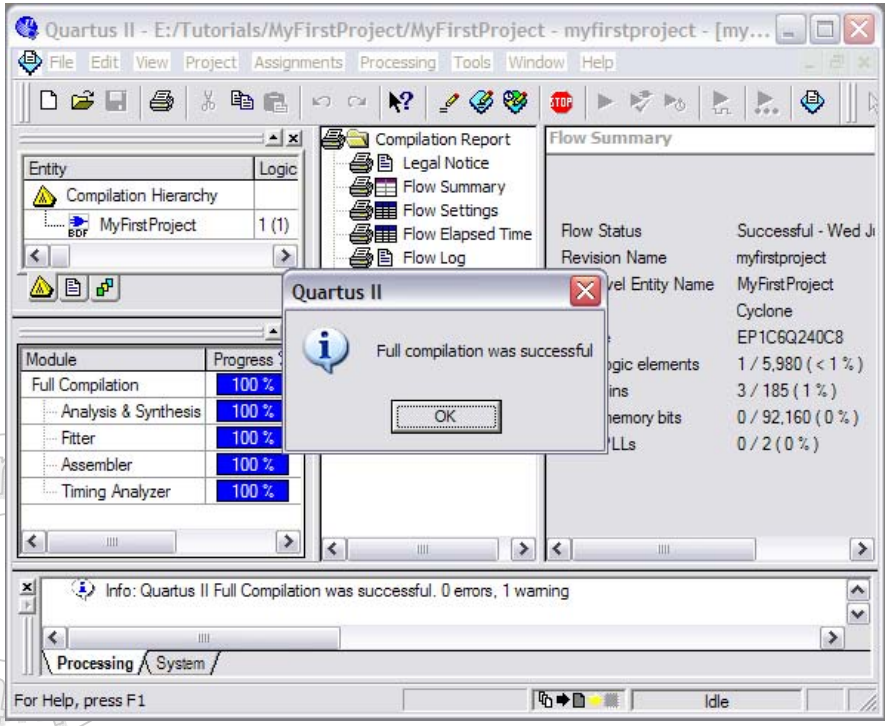
FIGURE 18. Compilation Status



After compilation completes a message will appear indicating Full Comilation was sucessfull.

9. Click **OK** to close the window

FIGURE 19. Final Compilation



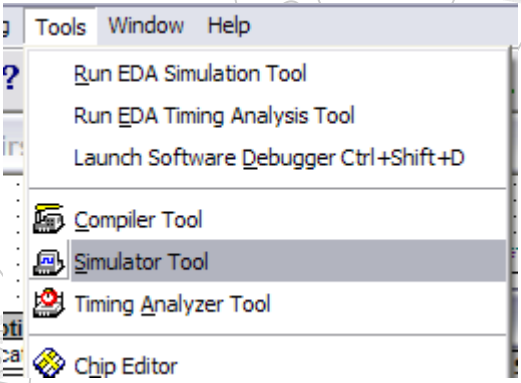
Notice a few things, the Flow Summary on the right hand side shows the details of the project. After compilation, the design requires only 1 Logic Element (LE) and 3 pins. Remember, in schematic entry, 1 DFF was instantiated so this translated into 1 LE. Furthermore, 2 input pins and 1 output pins were assigned; hence, a total of 3 External I/O pins.

Section 4: Simulation

Quartus II ships with an in-built simulator which may be used to stimulate the design and view the outputs before checking functionality in hardware. By using the simulator first, one gains confidence in the proper functioning of the design. Below are step by step instructions on using the simulator in the context of this tutorial.

1. Envoke the simuation tool by click **Tools** in the menu bar and then **Simulator Tool** as in Figure 20 below.

FIGURE 20. Envoke Simulator

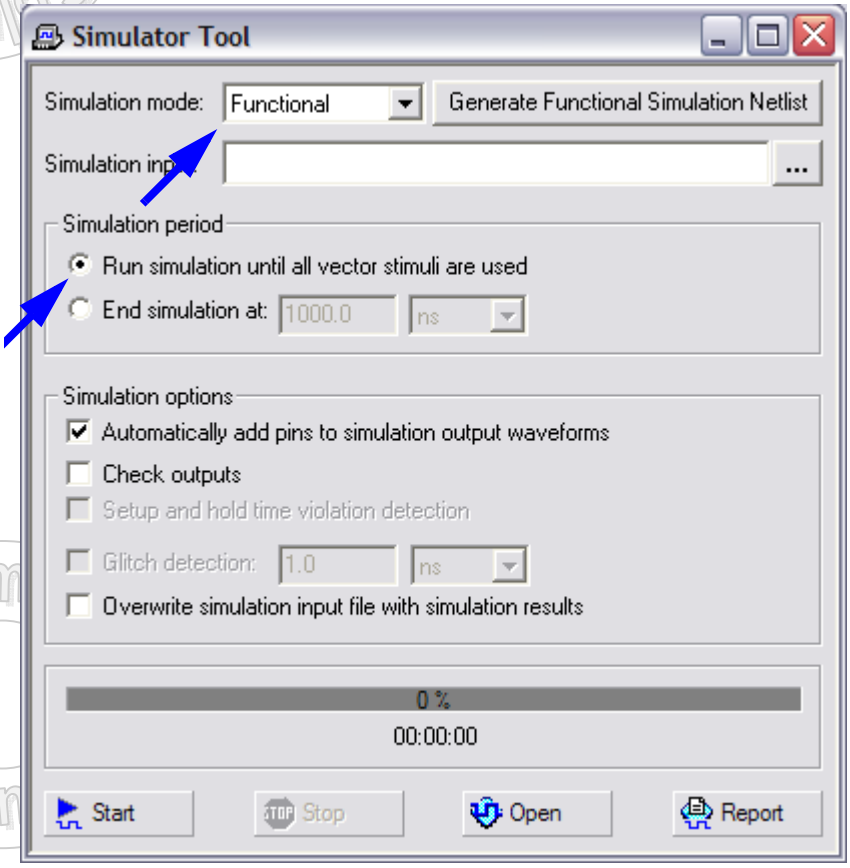


When the simulator tool appears, a number of items must be changed.

2. At the top next to **simulation mode**, click on the drop-down box and **change from timing to functional**
3. Under **simulation period,** click on the radio button for **Run simulation until all vector stimuli are used**.
4. Now at the bottom, click on **Open**

Figure 21 shows the final configuration before clicking on **Open**

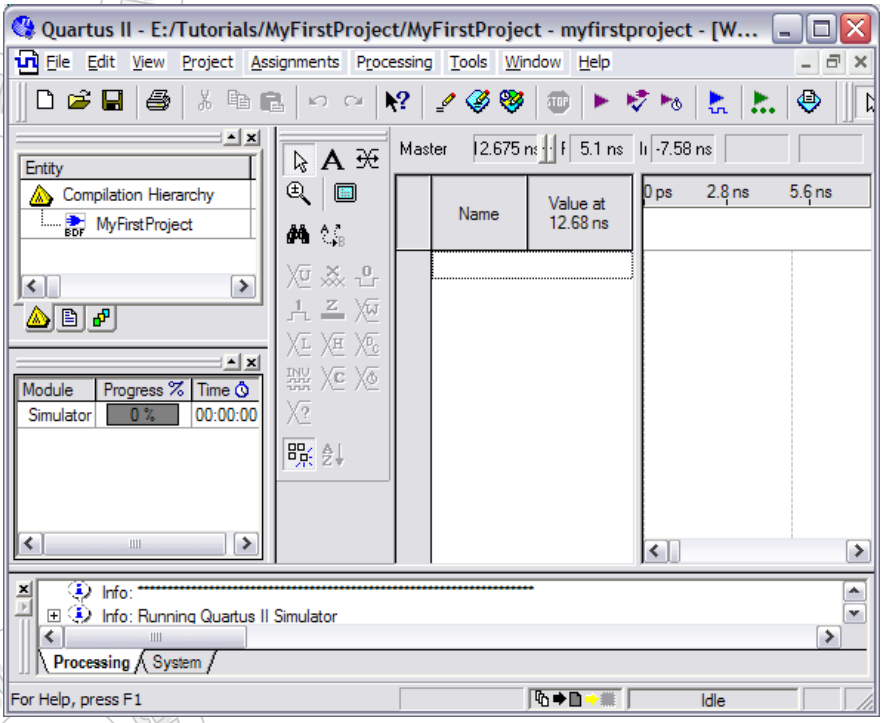
FIGURE 21. Simulator Tool



Note that the simulator tool may be maximized so that the following waveform window which opens is also maximized.

5. If the waveform window isn't maximized, then click on the **maximize window** button on the upper right corner of the window. This will make the look project less cluttered. Figure 22 shows the result.

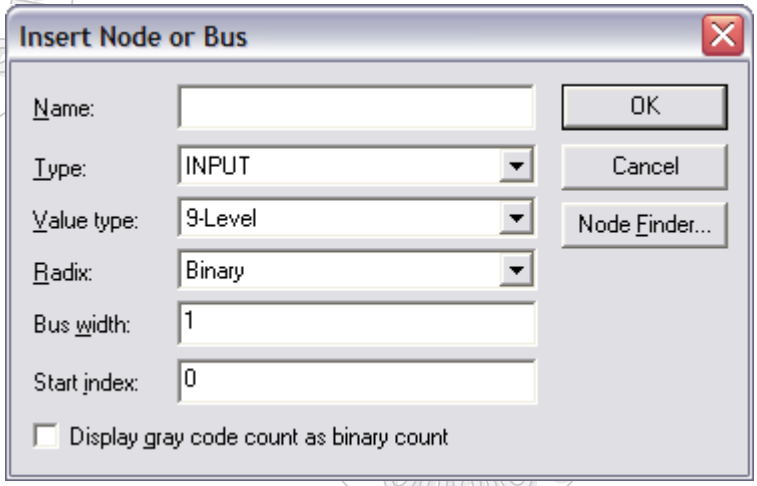
FIGURE 22. Simualtion Waveform



Now signals must be added and waves created in order to simulate the design.

6. Invoke the Node insertion tools by going into the window that contains the **Name and Value and Double click**. This opens the window as shown in Figure 23.

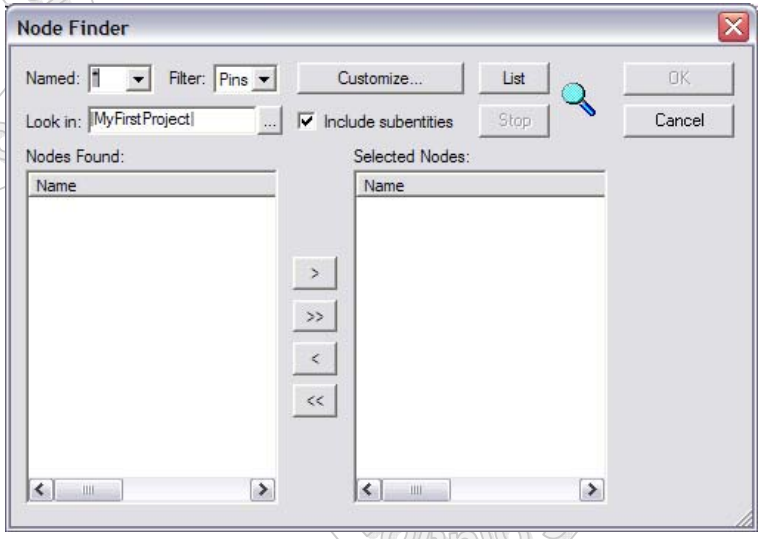
FIGURE 23. Add Node



7. Click on **Node Finder**

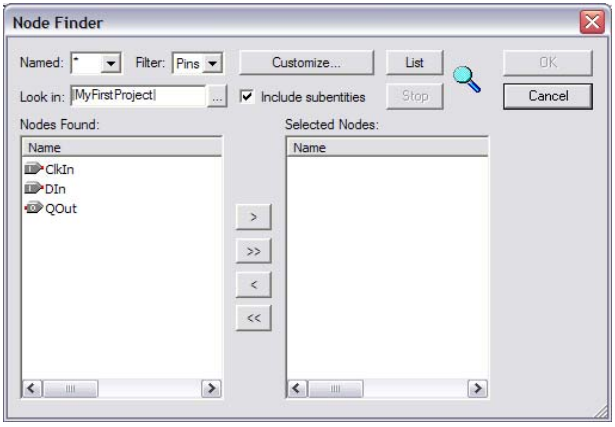
This causes a new window to pop-up as shown in Figure 24.

FIGURE 24. Node Finder



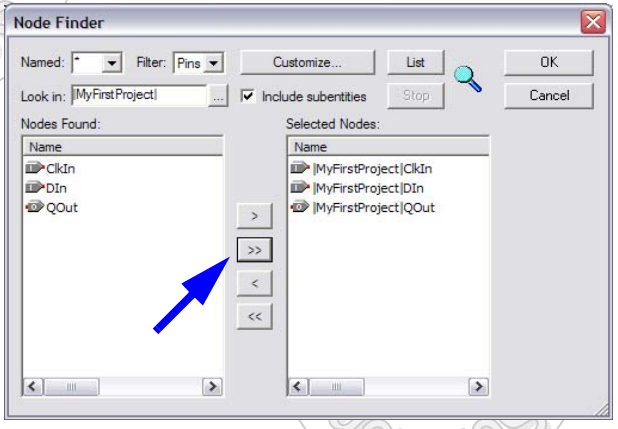
8. Near the magnifying glass, click on **List**. Notice in Figure 25 under **Nodes Found**, the DFF pins are seen ClkIn, DIn, and QOut.

FIGURE 25. Nodes Found



9. Select the Nodes. For example, **double click on ClkIn** and notice it will be moved to the Selected Nodes side. **Repeat** this for the rest of the nodes. Another way to perform the operation is to click on the **">>"** arrow. Figure 26 shows the final result.

FIGURE 26. Nodes Selected

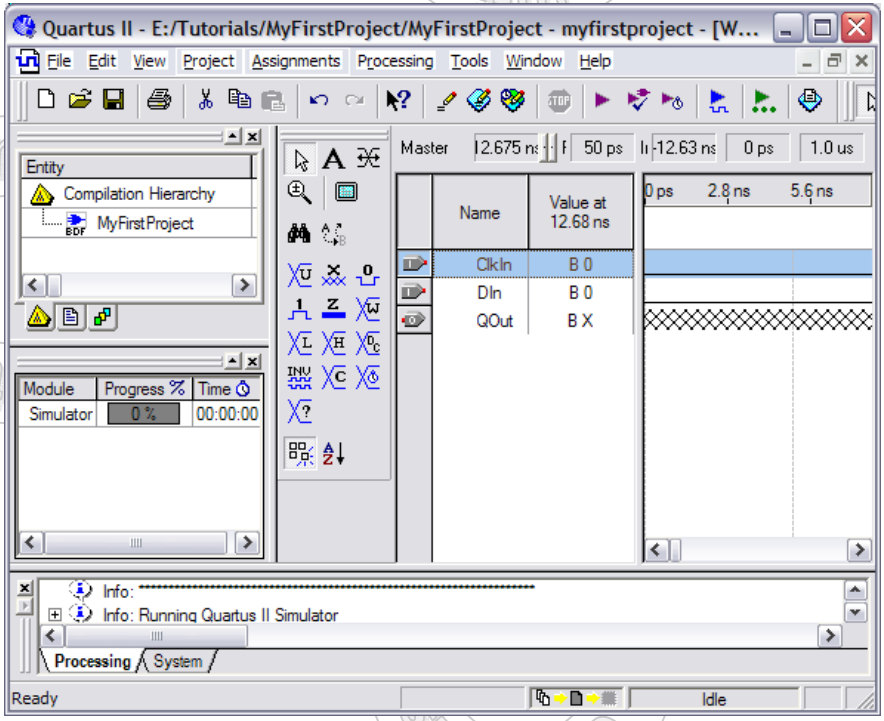


10. Now finish up by clicking on **OK** for the Node Finder Dialog.
11. Then click **OK** for the Insert Node or Bus Dialog.

The selected nodes are displayed on the Name window and default waves are shown. Notice for QOut, the display shows XXX's. Since the simulation has not occured no output is shown. However, for the default inputs the output will not be to interesting. Below are steps to change the input stimulus.

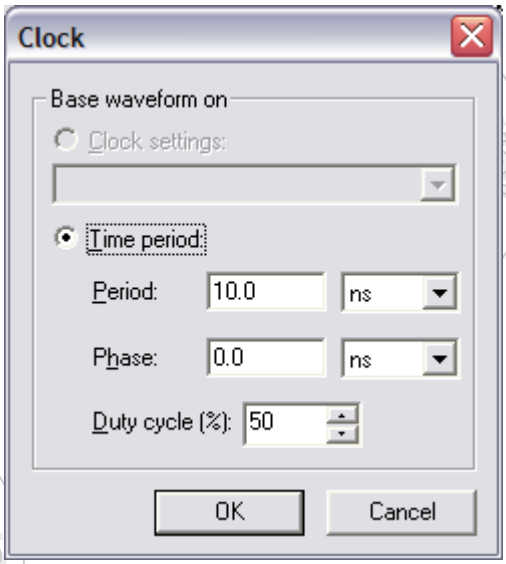
12. **Single Click on ClkIn** and notice the ClkIn line is highlighted in light blue and addition icons are enabled in the simulation tool-bar on the left as show in Figure 27.

FIGURE 27. Select ClkIn



13. For ClkIn a clock type waveform needs generation. This is simply accomplished by **clicking on the Overwrite Clock icon**  causing the Clock dialog to pop up as shown in Figure 28.

FIGURE 28. Clock Dialog.



14. **Change the Period** from 10.0 to 20.0, then click **OK**. Notice that a clock waveform has been added.
15. Now create a waveform like one shown in Figure 29 using the waveform icons. In the waveform area, first select the area to edit and then click on an icon.

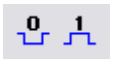
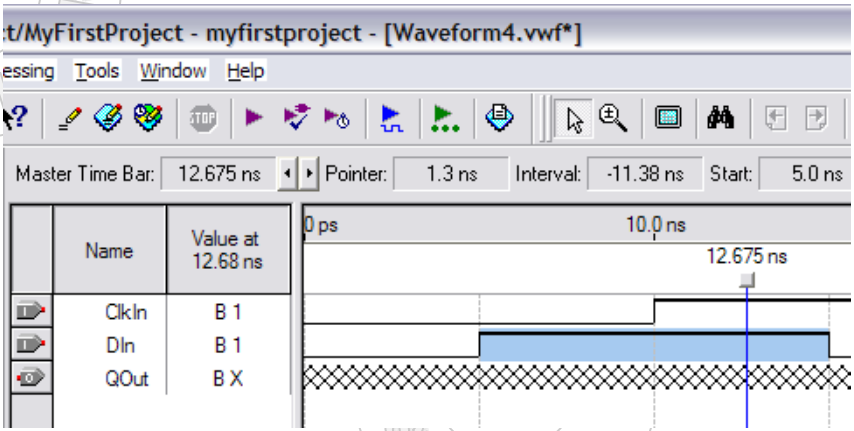
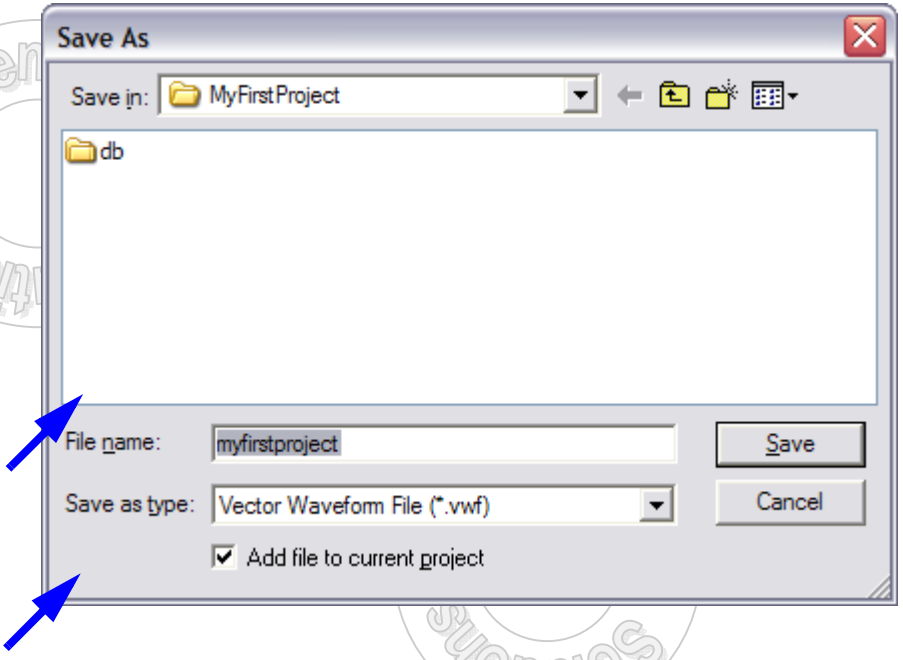


FIGURE 29. Simulation Waveforms



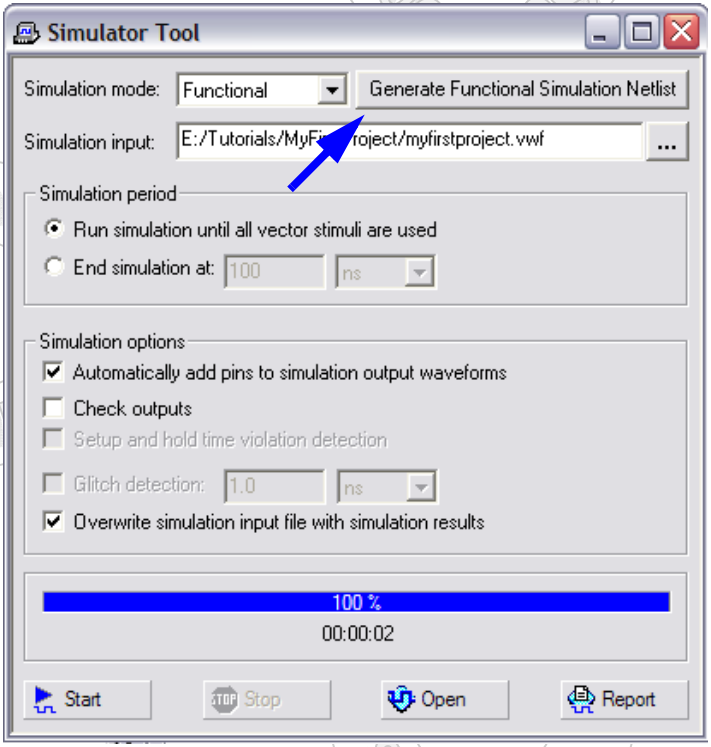
16. Now that the waveforms are created first **Save** the file.

FIGURE 30. Save Waveforms



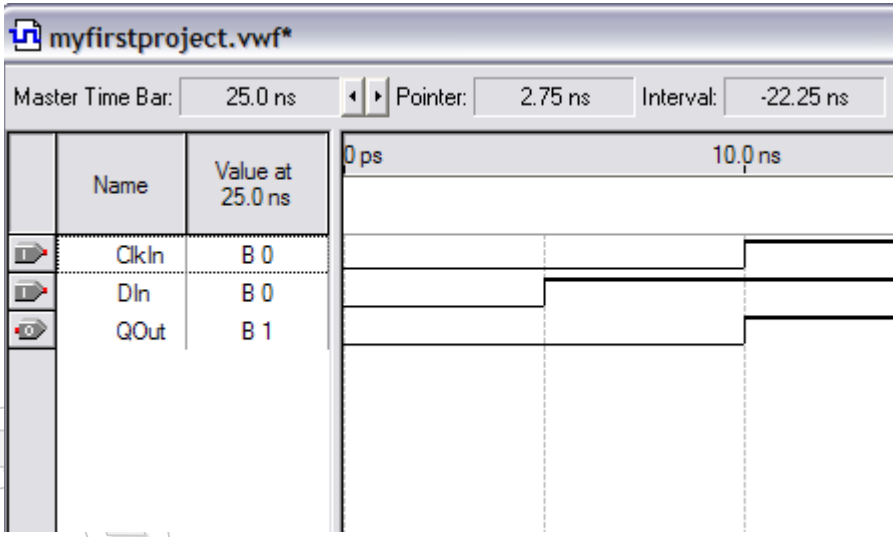
17. The file name is automatically set to myfirstproject so click on **Save**. Make sure that the “Add file to current project” check box is checked
18. Now go back to the Simulator Tool by **Tools -> Simulator Tool**. then Click on **Generate Functional Simulation Netlist**. Once complete and successful click **OK**. Then go back to the Simulation Tool.
19. Click on the check box for **Overwrite simulation input file with simulation results**.
20. Now start the simulation by clicking on the **Start** button. Once simulation is successful, click **OK**. The Simulation Tool dialog will look like Figure 31 showing 100% completion.

FIGURE 31. Simuation Tool after Starting



21. Now bring focus to the myfirstproject.vwf window and view the results. Notice that the QOut waveform has been created according to the DFF function. Notice that there are no FPGA delays. The output is seen immeadiately on the rising edge of the ClkIn. See Figure 32.

FIGURE 32. Simulated Waveform Output



22. Now play with the rest of the tool bar icons to Zoom In/Out and Change the inputs.
23. To simulate again simply click on the **Start Simulation** icon or use the Simulation Tool.

24. Now in the **Simulation Tool** change the simulation mode to Timing and click on Start. Now the myfirstproject.vwf window will show delays that are incurred. Use the tools to see that the ClkIn to QOut delay is 6.91ns.

Section 5: Programming the FPGA

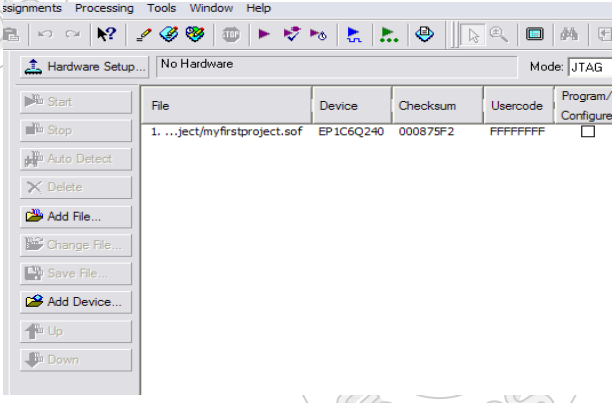
Compilation generates a number of files; but, the files to use to programming the FPGA are either the .sof or .pof files. Hence, there are two ways to program the Cyclone FPGA on the board.

- JTAG programming mode. In this mode, only the .sof may be downloaded while the system is powered. Once the system is powered down, the FPGA will lose it's programming.
- Active Serial mode. This mode produces a more permanent result using the .pof file. An Altera EPROM is programmed and upon power-up the FPGA will be programmed with the contents in the EPROM.

Before setting using the mode first the programming hardware must be configured. The step below show how.

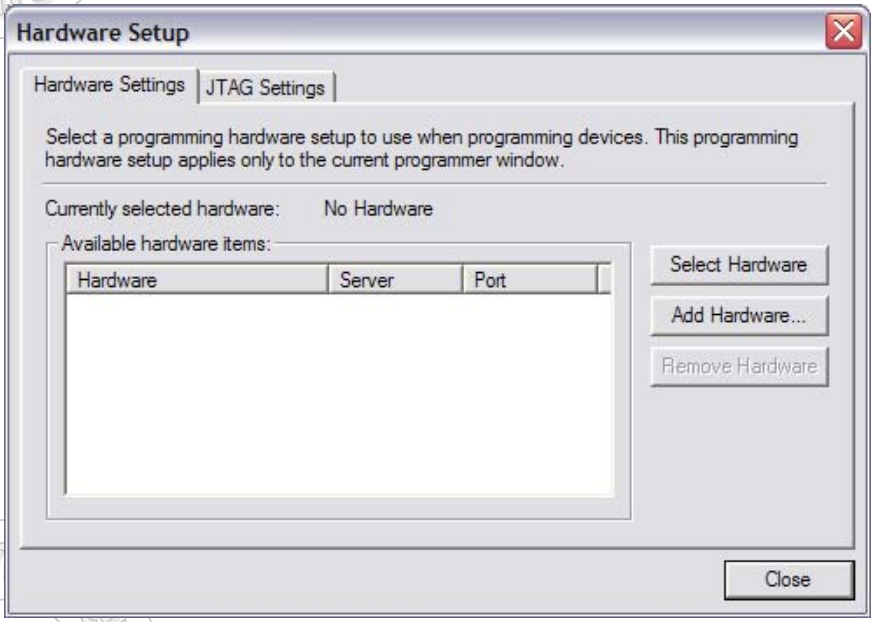
1. Choose **Programmer** from the Tools menu. A new Chain Description file (.cdf) opens in the Programmer window automatically listing the myfirstproject.sof file as the current programming file with the mode selected as JTAG and hardware setup set to No Hardware. As shown in the Figure 33.

FIGURE 33. Programming Window



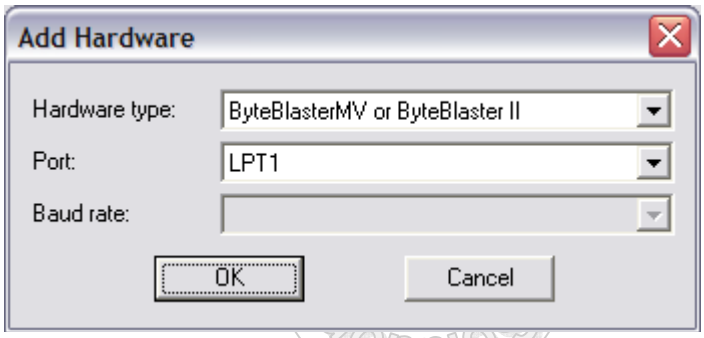
2. Click on the **Hardware Setup** button. The hardware setup dialog box pops up as shown in Figure 34.

FIGURE 34. Hardware Setup



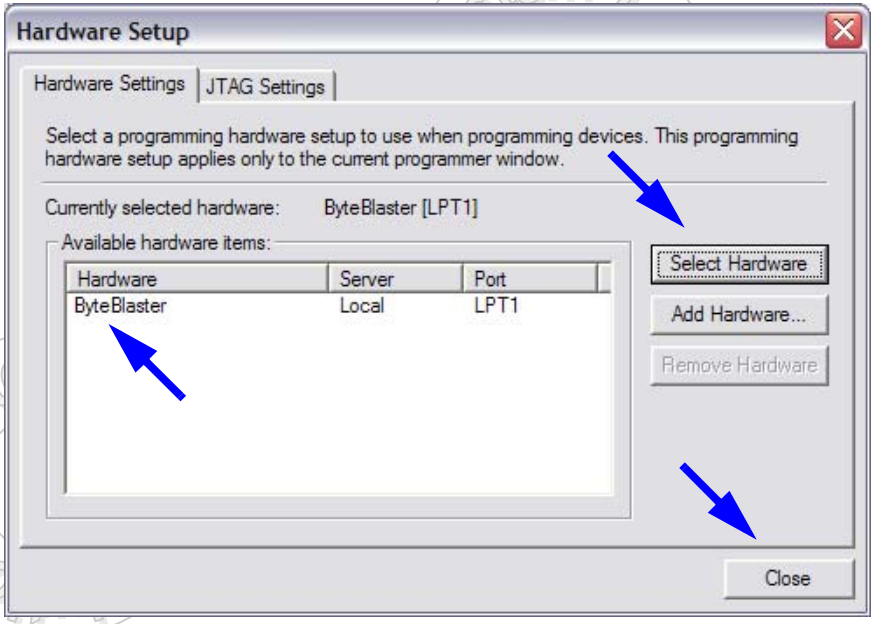
3. Click on the **Select Hardware** button. Figure 35 shows the dialog box

FIGURE 35. Add Hardware



4. Select the type of hardware from the drop down list and also select the port. Then click on **OK**.
5. Now under the Available Hardware Items, the hardware type is seen. In this example it is ByteBlaster. Click on the **Byte-Blaster** and then click on **Select Hardware**.
6. Now under the Currently selected hardware: ByteBlaster[LPT1] is seen as shown in Figure 36. Click on **Close**.

FIGURE 36. Selected Hardware



The hardware is now setup and progamming can occur.

Note: Make sure the programming hardware is connected to the computer to proceed with the next steps.

JTAG programming

1. Make sure that the mode type selected is **JTAG**. See the upper-right side of Figure 33.
2. Click on the **Program/Configure** check box as shown in Figure 37.

FIGURE 37. JTAG Programming

3. Connect the Byte Blaster Cable to JTAG connector header (JP12) on the board.
4. Click **Start** as shown in Figure 37 to program the FPGA.

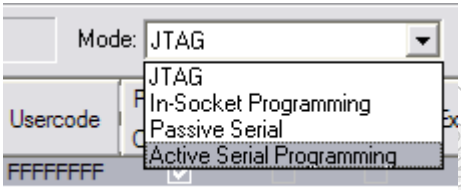
As soon as the programming starts, percentage will get displayed in the Progress bar. After it reaches 100%, the Config done LED will glow on the board.

The FPGA is now programmed and now using the Push Button and DIP Switch, the DFF functionality may be implemented to turn on and off the LED. Skip to Section 6.

Active Serial Mode Programming

1. Select Mode as **Active Serial Programming** as shown in Figure 38.

FIGURE 38. Select Active Serial Programming



2. When switching over from JTAG to ASP, a dialog box like one shown in Figure 39 ask to clear all devices. Click **Yes**.

FIGURE 39. Change Dialog

3. Now Select **Add File** to add the myfirstproject.pof to the file list. See Figure 40.
4. Now the Select Programming File dialog box appears so select **myfirstproject.pof** and click **Open**. Now the .pof file is added to the file list. Figure 41 shows the details.

FIGURE 40. Select Add File

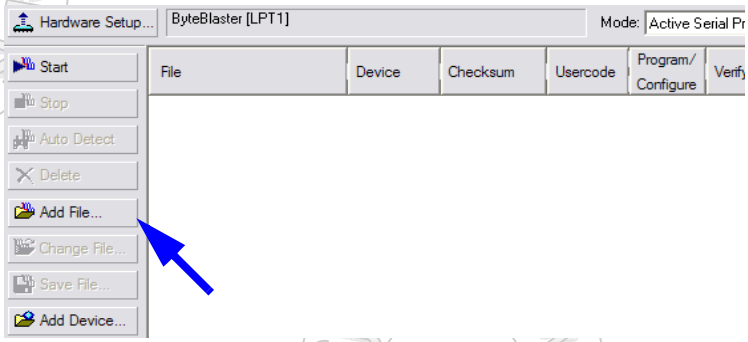
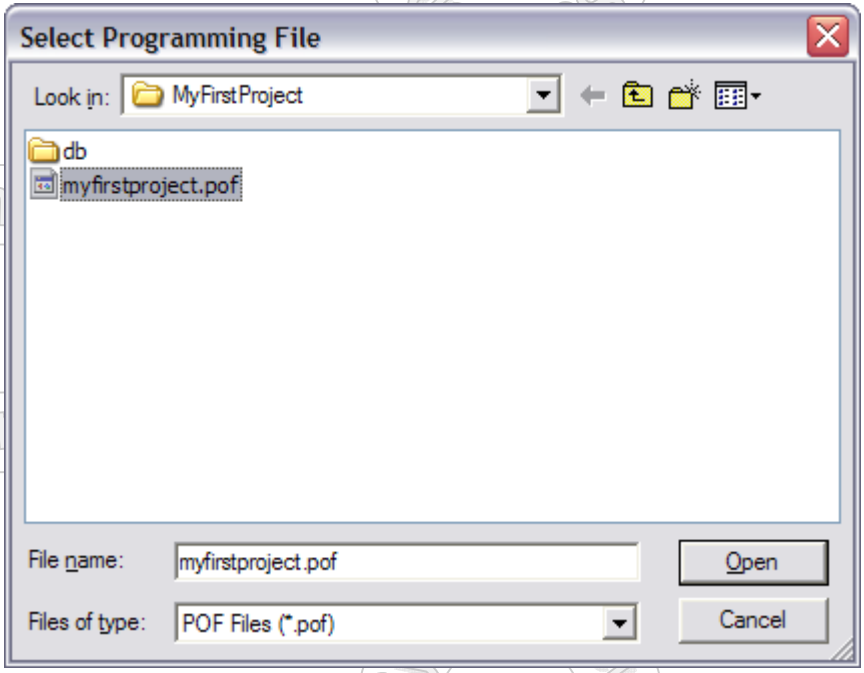


FIGURE 41. Select POF File



8. Click on the **Program/Configure** check box as shown in Figure 37.
9. Connect the Byte Blaster Cable to Active Serial header (JP11) on the board.
10. Click **Start** as shown in Figure 37 to program the FPGA.

Note: While downloading .pof file, if some error occurs then check that the selected configuration device is EPCS1. In order to do this, select Settings under Assignments menu, Click on Device & Pin Options. Under General option select Generate Compressed bit-streams option. Then select Configuration option. Under that select the Configuration Scheme as Active Serial. Select the Configuration Device as EPCS1. See section 3 Figure 16 and 17 as well as the associated text.

Now the EPCS1 EPROM has been programmed so each time the board is powered the myfirstproject design will be loaded into the FPGA.

Section 6: Using the Hardware

Testing the design is very easy to perform as all the components are found on the lower left corner of the board. Make sure the board has been programmed with either mode.

Note: When the board is first programmed, the D3 LED does not glow. **Since the LEDs are active high, they glow only when a "1" is provided**. **Also note that on the DIP Switch the "On" position provides a "0" to the FPGA**. See the board reference manual for more information.

1. Find Push Button SW4
2. Find DIP Switch SW3 Postion 1
3. Find LED D3
4. Toggle DIP Switch SW3 Postion to the OFF position if not already there.
5. Press Push Button SW4
6. The LED D3 will turn On.
7. Toggle the DIP Switch and press the Push Botton to turn On and Off the LED.

   Remember the Push Button generates an edge for the DFF as it is connected to ClkIn and the DIP Switch is the DIn.

NOW EXPERIMENT!!!!