

Schematic D-Flip Flop

Tutorial One

Version 1.0











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System Level Solutions





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Introduction

This tutorial will guide one through the basic features of the Quartus II software. It explains how to design, compile, simulate and program your logic designs in the Quartus II software using a D-Flop.

A design using a D-Flop will be created and assigned FPGA pins according to the UP3 board layout. In this particular case, the D input will be controlled by a DIP switch, the CLK input will be controlled by a Push-Button Switch. The output Q shall be assigned to an LED so that the functionality may be visually observed.

Start Lesson Section 1: Project Creation

The Quartus II software offers a New Project wizard to help create a new project. The project settings may be changed using menu commands and dialog boxes. To create a new project using the New Project Wizard, follow the steps below:

1. Choose New Project Wizard (File menu). The New Project Wizard appears as shown in Figure 1. Opening the New Project Wizard for the first time may display the Introduction page; click Next to proceed to the first page of the wizard.

Click on the check box "**Don't show...**" to disable the dialog box from appearing the next time the wizard is run.



R	New Project Wizard: Introduction	×
	The New Project Wizard helps you enter settings that apply to your entire project, including the following:	,
	 Project name and directory Name of the top-level design entity Design files, other source files, and libraries to be used in the project Device and family to be used for compilation EDA tool settings 	
	You can change the settings for an existing project and specify additional project-wide settings with the Settings command (Assignments menu). You can use the various pages of the Settings dialog box, including the Timing Settings, the Default Parameter Settings, and the Default Logic Option Settings pages, to add functionality to the project.	
	Don't show me this introduction again	
(3)	Back Next Finish Cancel	

In either case, click Next

A new dialog box, as shown in Figure 2, appears asking for working directory and related information.

2. Type the directory name in the working directory box, or select the directory with **Browse** (...).

•••

•••

...

It is a good idea to create a new directory to encapsulate the design. So within the Tutorial directory create a new directory called **MyFirst-Project**. (Click on the folder with a star).

- 3. Type a name for the project in the project name box. If not automatically entered for by the tool, then for this example, type **MyFirstProject**.
- 4. Type **MyFirstProject** as the name of the top-level design entity of the project in the top-level design entity box.

This must be the exact name of the top-level module.

5. Click Next

FIGURE 2. Top Level Entry

New Project Wizard: Directory, Name, and Top-Level Entity [page 1 of 6]	×

What is the working directory for this project? This directory will contain design files and other related files associated with this project. If you type a directory name that does not exist, Quartus II can create it for you.

E:\Tutorials\MyFirstProject

What is the name of this project? If you wish, you can use the name of the project's top-level design entity.

MyFirstProject

What is the name of the top-level design entity in your project? The Quartus II software will automatically create Compiler and Simulator settings for the top-level entity you specify in this wizard. After you create a project, you can add more top-level entities and create Compiler and Simulator settings for them with commands on the Assignments menu.

MyFirstProject

Back	Next	Finish	Cancel
	^o lin	03	



6. The **Add Files** page appears as shown in Figure 3. In this particular case, no design files pre-exist. However if the design files already existed for the project, simply click on **Browse** (...) to select the appropriate files, and then click **Add** to add them to the project.

FIGURE 3. Add Files

Eile name:		•••	Add
File name		Туре	Add A
			<u>R</u> emov
			Propert
			Цр
			Dowr
If your project include pathnames:	es libraries of custom funct	ions, specify their	

7. Click Next

The **EDA Tool Settings** page dialog, as shown in Figure 4, appears. This page allows one to specify options for other EDA tools for use with this project. Since this project does not use any other EDA tools, make sure that **None** is specified in the **Tool name** column for each tool type.

FIGURE 4. EDA Tool Setting

EDA tools					
Tool type	de e sis	Tool name <none></none>			
Design entry/syn Simulation	ithesis	<none></none>			
Timing analysis		<none></none>			
Board-level Formal verificatio	n	<none> <none></none></none>			
Resynthesis	"	<none></none>			
- Tool settings					
Tool type:	Design entry	/synthesis			
Tool name:	<none></none>				
🔲 Run this too	l automatically	y to synthesiz	e the current	design	Se
					Ad
					80

Click Next



8. The next dialog box, as shown in Figure 5, asks for specific information related to the hardware. Select the target family. Since the board uses a **Cyclone** device, select the Cyclone family. Then select the **YES** button, to target a specific device, namely the **EP1C6Q240C8** on the shown in Figure 6.

FIGURE 5. Device Family

l	New Project Wizard: Device Family [page 4 of 6]	×
	Which device family do you wish to target?	
	Eamily: Cyclone	
	Do you want to assign a specific device?	
	 Yes No Lowenths allow the Constitute shares a device 	
	○ No, I want to allow the Compiler to choose a device	
a		
S		
2014		
R		
Ûa		
		-
	Back Next Finish Cancel	

- 9. Click Next.
- 10. Scoll down the list or use the package, pin or speed grade drop down boxes to select the part. Again, select **EP1C6Q240C8**.

devices" list. Select a device in the Available devices: EP1C4F324C6 (Advanced) EP1C4F324C7 (Advanced) EP1C4F324C8 (Advanced) EP1C4F400C6 (Advanced) EP1C4F400C7 (Advanced) EP1C4F400C8 (Advanced) EP1C4F400C8 (Advanced) EP1C6F256C7 EP1C6F256C7 EP1C6F256C7 EP1C6F256C7 EP1C6F256C8 EP1C6F256C8 EP1C6F256C8 EP1C6F256C8	e devices that are displayed in the "Available	X
EPIC60240C8 EPIC6T144C6 EDICCT144C7 Ba	▼ ack Next Finish Cance	əl

The last dialog box, as show in Figure 7, displays the **Summary** for the entire project.



-) W	FIGURE 7. Project Summa	-	X
		ect will be created with the following settings:	
	Project directory: e:\tutorials\myfirstproject\		
	Project name:	MyFirstProject	
	Top-level design entity:	MyFirstProject	
	Number of files added:	0	
	Number of user libraries added:	0	
	EDA tools:		
	Design entry/synthesis:	<none></none>	
	Simulation:	<none></none>	
	Timing analysis:	<none></none>	
	Board design:	<none></none>	
	Device assignments:		
	Family name:	Cyclone	
	Device:	EP1C6Q240C8	
(S)			
(DY)		Back Next Finish	Cancel
1 CP			
140	Man O'e		
	E U U		

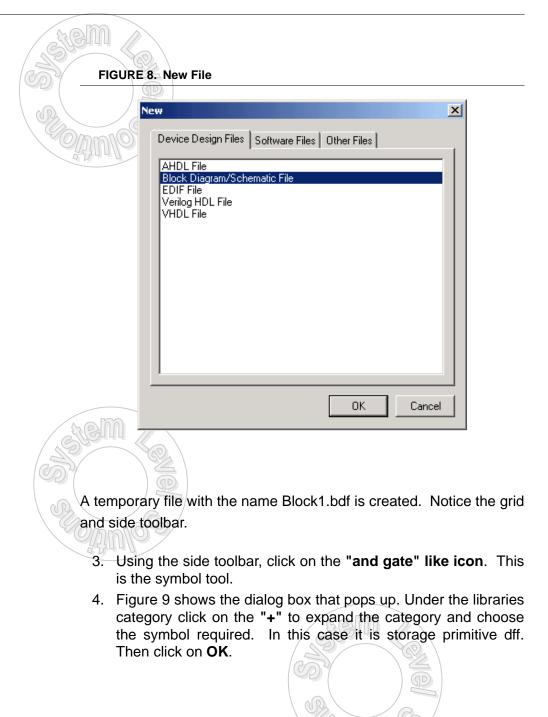
Section 2: Schematic Entry

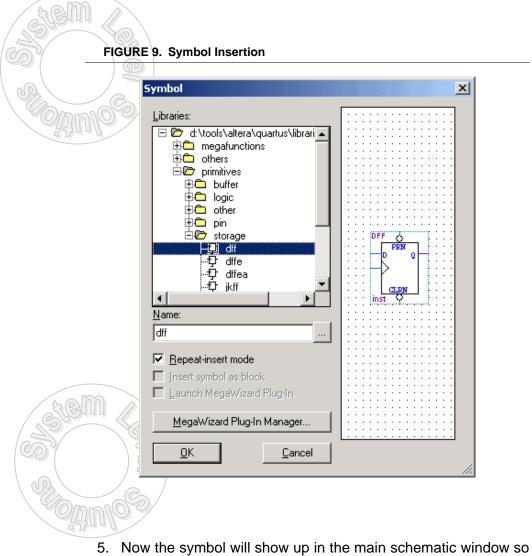
After creating the project, the design must be entered. Quartus II allows a number of methods of design entry. Completion of the following steps will show how to create a schematic and include it in the project. The objective is to instantiate a D-flop and assign it to the proper pins.

- First create new file by File -> New ... or simply clicking on the new file icon.
- 2. As Figure 8 shows below, select **Block Diagram/Schematic** File then click **OK**









- simply move the symbol to the desired location and **left click.**
- 6. After placing one instance, click on the "arrow" icon in the vertical toolbar or press **ESC**.
- 7. Repeat Step 4.
- 8. This time choose primitive pin input. Click OK.

- 9. Place two instances of the input--one for the D input and the other for the Clk(shown as a greater than sign). Make sure that the newly placed instances touch the dff inputs. If not the input primitives may be connected using the Orthogonal Node Tool found on the left vertical tool bar.
 - 10. Repeat Step 4
 - 11. Choose primitive pin output. Click OK.
 - 12. Place the output pin instance on Q. Then press ESC.
 - 13. To zoom in or out use the Zoom Tool.
 - 14. Before proceeding, it is a good idea to save the diagram.

File -> Save ... or simply clicking on the save file icon.

15. Below, Figure 10 shows the dialog box. Make sure that "Add file to current project" is checked. The file name field is prefilled with MyFirstProject which is the name of the entire project. Keep this name as the default. Click **Save**. As an exercise after completion of this tutorial, use a different name and observe what happens.

FIGURE 10. Save Dialog

	Save As				
Le le		MyFirstProject	- ← 6	. 💣 🎟 -	×
	🛅 db				
Con Contraction					
~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~~					
20111	File <u>n</u> ame:	MyFirstProject		<u>S</u> ave	ו
	Save as type:	Block Diagram/Schematic File (*.bdf)	•	Cancel	
		Add file to current project			11.

16. The instantiated primitives need unique names. Double Click on the **DFF primitive** after which the following dialog box appears (Figure 11). Change the instance name field to **DFIop** and Click **OK** 

Another way is to double click on the instance name directly and change it there.

ACH	n 📐							
	FIGURE 11.	Symbol Pr	operties					
<u>G</u>	I I	-						
R	Symbol Propert	ie <i>s</i>						×
KOM	General Ports	Format						
4	Symbol <u>n</u> ame:	DFF						
	Instance name	e: D-flop						
	-							
46								
( 59 m								
S						OK	Cance	<u> </u>
	17. Repeat	step 17 DIn and		input prin	nitives	with tl	he follo	wing
							ha falla	
4	18. Repeat name: 0	•	for the	output prir	nitives	s with t	ne tollo	wing
	Now for the r	nost impo	rtant part-	the assign	ment	of the de	esign pir	ns to
	the physical	FPGA pi	in locatio	n. In the	boar	d refere	nce ma	nual
	please refer	to the sec	tions on F	Push Butto	n Swit	ches, D	IP Switc	hes,
				C/DM	106			

and LEDs. The named pins must be assigned as specified in the table below.

TABLE 1. Board Connectivity

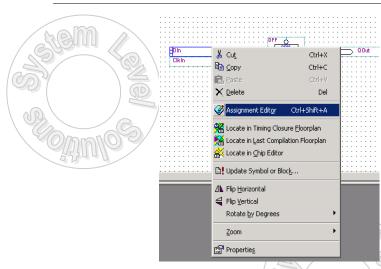
2	Design Pin Name	FPGA Assignment	Board Function
	DIn	Pin 58	DIP Switch-SW3.1
	ClkIn	Pin 48	Push Button-SW4
	QOut	Pin 56	LED-D3

## Confirm the above by looking at the reference manual.

The pin assignment editor may be invoked in multiple ways.

19. As an example, **Right Click on Dln** and select **Assignment Editor**. Figure 12 shows the invoked dialog box.

### FIGURE 12. Pin Assignment



Another way is to select the DIn input pin and enter **Ctrl+Shift+A**. And yet another way is to select the DIn input pin and then from the

e opp	115	GURE 13	-	nent Editor					X
		Category:	All		• 🗘	All 🗈 Pin	👌 Timing	Logic Options	5
		🛛 🔽 Show as	signments for	specific nodes:					
	Node		DIn					Check All	
								Uncheck All	
	riller:							Delete All	
									_
de	×  ]]	Edit:	XV				r		
Stel			ame (From)	Destination N	ame (To)	Option	Va	lue	
	1 Thi: with	S is a <u>ver</u>	lame (From) ∠ busy w since th	◆ DIn indow. The intention	nere are	e many t	hings that	at can be doi pin number	

ø	Ass	ignment Ed	itor				_ 🗆 ×		
×	+	Category:	Pin		All 🕞 Pin 💍 Timi	ing 🔹 Logi	c Options		
N M		Show	gnments for s	pecific nodes:					
	ş		DIn			Ch	eck All		
Ш	Node Filter:					Und	heck All		
Ш	ter:					Del	lete All		
H									
	Information:		ntities to pins o Pins dialog box.	r regions on the device. I	for additional pin assignm	ient options, go	o to		
×		Edit:		n					
	7	Name		Location	I/O Bank	I/O Standard			
1		🔷 DIn							

21. In the Edit section, Double Click on **Location** and a drop down menu like Figure 15 appears. Select Pin_58 for Dln.

FIGURE 15. Pin L	ocation				
Show assignme	ents for specific nodes:				
				Check All	
	Pin_47	I/O Bank 1	Row I/O	LVDS4n	
$\mathcal{I}(\mathcal{O})$	Pin_48	I/O Bank 1	Row I/O	LVDS3p/DQ0L4	
	Pin_49	I/O Bank 1	Row I/O	LVDS3n/DQ0L5	
47444	Pin_50	I/O Bank 1	Row I/O	DPCLK0	
	Pin_53	I/O Bank 1	Row I/O	LVDS2p/DQ0L6	
signs a location	n on the d Pin_54	I/O Bank 1	Row I/O	LVDS2n/DQ0L7	
	Pin_55	I/O Bank 1	Row I/O	VREF2B1	
	Pin_56	I/O Bank 1	Row I/O		
	Pin_57	I/O Bank 1	Row I/O	LVDS1p	
	Pin_58	I/O Bank 1	Row I/O	LVDS1n	
	Pin_59	I/O Bank 1	Row I/O	LVDS0p	
	Pin_60	I/O Bank 1	Row I/O	LVDS0n	
	V Pin_61	I/O Bank 4	Column I/O	LVDS71p	
	Pin_62	I/O Bank 4	Column I/O	LVDS71n	
Name	Pin_63	I/O Bank 4	Column I/O	LVDS70p	-
DIn		-			
· · · · · · · · · · · · · · · · · · ·		10	04		

- 22. Then Click on Name for the Editor to accept the selection
- 23. Close the assignment editor window.

- 24. A message will pop asking to save. Click Yes
- 25. Another message stating messages generated during save pops up. Click **OK**
- 26. Repeat Steps 20 thru 26 for the rest of the pins.

## **Section 3: Compilation**

The Quartus II software allows compilation of an entire design, or any constituent part of a design. The "compilation focus," which is the design entity needing compilation, may be selected from any portion of the project hierarchy.

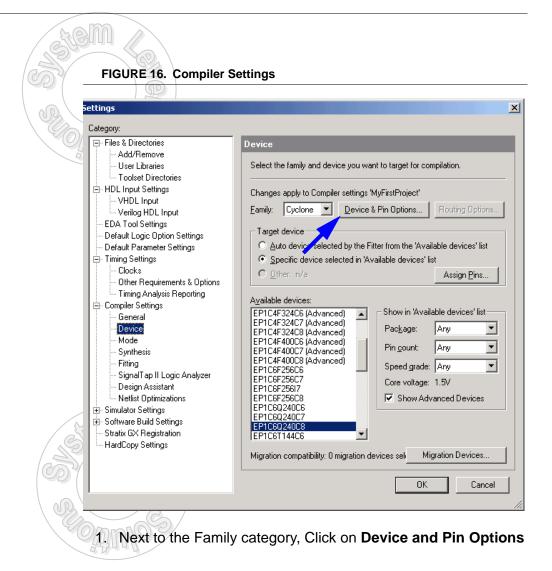
 Before actually compiling the design, one should set the appropriate Compiler settings by pressing Ctrl+Shift+E or on the menu bar Assignments -> Settings. Please see Figure 16. Three major compiler settings are required and explained in the steps below.

•Generate a Compressed Bit Stream.

• Set Configuration Scheme to Active Serial and use Configuration Device EPCS1

• Since the Cyclone device on the board connects to many other ICs and Connectors, one should set the unused pins as tri-stated inputs. This will tri-state the unused FPGA pins such that it doesn't drive other logic and potentially causing large currents to flow.





Now a new window will pop up allowing changes for some advanced configuration operations. Figure 17 shows the dialog.



Sem (
FIGURE 17. Device and Pin Options
Device & Pin Options
General Configuration Programming Files Unused Pins Dual-Purpose Pins Voltage Specify general device options. These options are not dependent on the configuration scheme.
Changes apply to Compiler settings 'MyFirstProject'
Options: Auto-restart configuration after error Release clears before tri-states Enable user-supplied start-up clock (CLKUSR) Enable device-wide reset (DEV_CLRn) Enable device-wide output enable (DEV_OE) Enable INIT_DONE output
Generate compressed bitstreams     Auto <u>u</u> sercode     JTAG user code (32-bit hexadecimal):     FFFFFFF Description:
Directs the device to restart the configuration process automatically if a data error is encountered. If this option is turned off, you must externally direct the device to restart the configuration process if an error occurs.
<u>R</u> eset
OK Cancel

- 2. Under the **General Tab**, click on the Generate compressed bitstreams check box.
- 3. Under the **Configuration Tab**, set the configuration scheme to **Active Serial**
- 4. Under the **Configuration Tab**, set the configuration device to **EPCS1**
- 5. Under the Unused Pins, select radio button As inputs, tristated

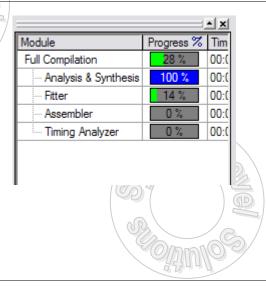
- 6. After completion of the above steps click **OK** to close the Device & Pin options diaglog
- 7. Then click **OK** to close the Settings dialog

Now the design is ready for acutal compiliation. Again, there are several access mechanisms to perform the compile option.

- •Use the standard quartus II tool bar and click on the Start Compliation icon
- •On the menu bar under Processing click on Start Compilation
- Press Crtl-L
- 8. For this tutorial Press Ctrl+L

The complier will start and the left side of Quartus should show the status. Full compilation consists of Analysis and Synthesis, Fitting, Assembling and Timing Analysis.

### FIGURE 18. Compilation Status



After compilation completes a message will appear indicating Full Comilation was sucessfull.

9. Click OK to close the window

FIGURE 19. Final Compilation

		k? 🦉 🏈 💖		<b>≿   ≿   @   </b>
Entity Compilation Hierarchy	1 (1)	Compilation Report Compilation Report Flow Summary Flow Settings Flow Elapsed Time Flow Log	Flow Summary Flow Status Revision Name	Successful - Wed Jr myfirstproject
Module F Full Compilation Analysis & Synthesis Fitter	Quartus	II Full compilation was su	ccessful ins nemory bits	MyFirstProject Cyclone EP1C6Q240C8 1 / 5,980 ( < 1 % ) 3 / 185 ( 1 % ) 0 / 92,160 ( 0 % ) 0 / 2 ( 0 % )
Assembler Timing Analyzer	100 % 100 %		<	
Info: Quartus II F     Processing ( System /	Full Compilation was s	uccessful. O errors, 1 wa	ming	× >

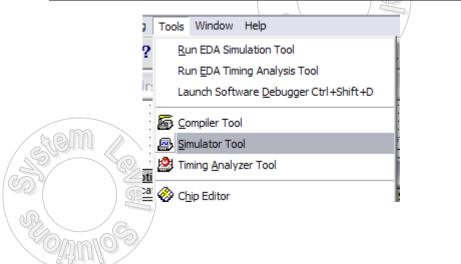
Notice a few things, the Flow Summary on the right hand side shows the details of the project. After compilation, the design requires only 1 Logic Element (LE) and 3 pins. Remember, in schematic entry, 1 DFF was instantiated so this translated into 1 LE. Furthermore, 2 input pins and 1 output pins were assigned; hence, a total of 3 External I/O pins.

## **Section 4: Simulation**

Quartus II ships with an in-built simulator which may be used to stimulate the design and view the outputs before checking functionality in hardware. By using the simulator first, one gains confidence in the proper functioning of the design. Below are step by step instructions on using the simulator in the context of this tutorial.

1. Envoke the simulation tool by click **Tools** in the menu bar and then **Simulator Tool** as in Figure 20 below.

FIGURE 20. Envoke Simulator



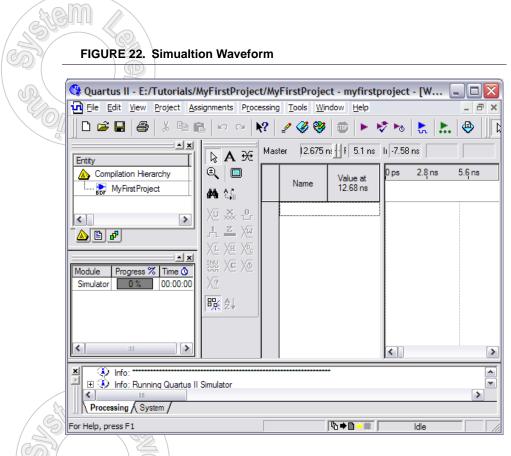
When the simulator tool appears, a number of items must be changed.

- 2. At the top next to **simulation mode**, click on the drop-down box and **change from timing to functional**
- 3. Under simulation period, click on the radio button for Run simulation until all vector stimuli are used.
- 4. Now at the bottom, click on Open

Figur	e 21 shows the final configuration before clicking on <b>Open</b>
FIC	GURE 21. Simulator Tool
<u>O</u> AN E	Simulator Tool
	Simulation mode: Functional  Generate Functional Simulation Netlist
	Simulation inp
	Run simulation until all vector stimuli are used     End simulation at: 1000.0     Ins
	Simulation options
	Automatically add pins to simulation output waveforms     Check outputs
200	Setup and hold time violation detection     Glitch detection: 1.0     Ins
Stani	Overwrite simulation input file with simulation results
	0 % 00:00:00
×0/2m	🔭 Start 💮 Stop 😲 Open 🥋 Report

Note that the simulator tool may be maximized so that the following waveform window which opens is also maximized.

5. If the waveform window isn't maximized, then click on the **max-imize window** button on the upper right corner of the window. This will make the look project less cluttered. Figure 22 shows the result.



Now signals must be added and waves created in order to simulate the design.

6. Invoke the Node insertion tools by going into the window that contains the **Name and Value and Double click**. This opens the window as shown in Figure 23.



Sem Fic	SURE 23. Add	Node	
R	Insert Node	or Bus	
2010	<u>N</u> ame:		OK
	<u>T</u> ype:	INPUT 💌	Cancel
	<u>V</u> alue type:	9-Level	Node <u>F</u> inder
	<u>R</u> adix:	Binary 💌	
	Bus <u>w</u> idth:	1	
	Start index:	0	
	🗖 Display gra	ay code count as binary count	
	·		7

7. Click on Node Finder

This causes a new window to pop-up as shown in Figure 24.

Node Finder		
Named: T Filter: Pin	Customize List	
Nodes Found:	Selected Nodes:	
TRAINC		
	>	
	<	
	<<	
<	>	>

8. Near the magnifying glass, click on **List**. Notice in Figure 25 under **Nodes Found**, the DFF pins are seen ClkIn, DIn, and QOut.

FIGURE 25. Nodes Found

Named: 💌 💌 Filter: Pins 💌	Customize	List	OK
ook in: MyFirstProject	Include subentities	Stop	Cancel
Nodes Found:	Selected Nodes:		
Name	Name		
IIP Clun IIP DIn @ QOUt	> >> < <		
<	<	>	

9. Select the Nodes. For example, double click on ClkIn and notice it will be moved to the Selected Nodes side. Repeat this for the rest of the nodes. Another way to perform the operation is to click on the ">>" arrow. Figure 26 shows the final result.

### FIGURE 26. Nodes Selected

Named: F	ilter: Pins 💌	Customize	OK
Look in: MyFirstProje	cti 🔽	Include subentities Stop	Cancel
Nodes Found:		Selected Nodes:	_
Name		Name	
ClkIn		MyFirstProject ClkIn	
DIn QOut		MyFirstProject DIn MyFirstProject QOut	
	>		
	>:		
	-		
<	>	<	
			h

- 10. Now finish up by clicking on **OK** for the Node Finder Dialog.
- 11. Then click **OK** for the Insert Node or Bus Dialog.

The selected nodes are displayed on the Name window and default waves are shown. Notice for QOut, the display shows XXX's. Since the simulation has not occured no output is shown. However, for the default inputs the output will not be to interesting. Below are steps to change the input stimulus.

12. **Single Click on ClkIn** and notice the ClkIn line is highlighted in light blue and addition icons are enabled in the simulation toolbar on the left as show in Figure 27.

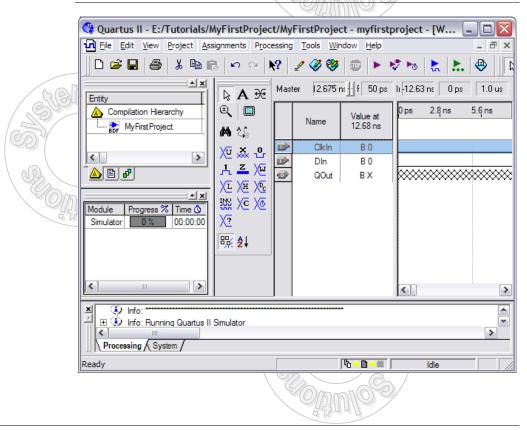


FIGURE 27. Select ClkIn

χø

13. For ClkIn a clock type waveform needs generation. This is simply accomplished by clicking on the Overwrite Clock icon

causing the Clock dialog to pop up as shown in Figure 28.

FIGURE 28. Clock Dialog.

Clock
Base waveform on C Clock settings;
✓ Time period Period: 10.0 ns ▼
P <u>h</u> ase: 0.0 ns 💌
Clock settings: ▼ Time period: Period: 10.0 ns ▼ Phase: 0.0 ns ▼ Duty cycle (%): 50 ★

- 14. Change the Period from 10.0 to 20.0, then click OK. Notice that a clock waveform has been added.
- 15. Now create a waveform like one shown in Figure 29 using the waveform icons. In the waveform area, first select the area to edit and then click on an icon.





Siem -	FIG	SURE 29. 3	Simulation	Waveforms			
R	t/My	FirstProje	ct - myfirst	project - [Wav	eform4.vwf*]		
(Omat	essing	<u>T</u> ools <u>W</u> ir			-		
4400	?	🦉 🏈 😻	1	🕏 🏍 🚼 .	k 🕘 🔤	₹ 🔲	M 🖲 🖻
	Mast	ter Time Bar:	12.675 ns	Pointer: 1	.3 ns Interval:	-11.38 ns	Start: 5.0 ns
		Name	Value at 12.68 ns	0 ps		10.0 ns	12.675 ns
		ClkIn	B 1				
		Dln	B 1				
	۲	QOut	ВX		**********	*****	

16. Now that the waveforms are created first Save the file.

FIGURE 30. Save Waveforms

hall	Save As		
Sterr	Save in: 🗀	MyFirstProject 💌 🗲 🗈 🖻	*
D'	db		
R			
~OM			
4.15			
	File <u>n</u> ame:	myfirstproject	<u>S</u> ave
	Save as type:	Vector Waveform File (*.vwf)	Cancel
		Add file to current project	
/			
·		201110.3	

- 17. The file name is automatically set to myfirstproject so click on **Save**. Make sure that the "Add file to current project" check box is checked
- Now go back to the Simulator Tool by Tools -> Simulator Tool. then Click on Generate Functional Simulation Netlist. Once complete and successful click OK. Then go back to the Simulation Tool.
- 19. Click on the check box for **Overwrite simulation input file** with simulation results.
- 20. Now start the simulation by clicking on the **Start** button. Once simulation is successful, click **OK**. The Simulation Tool dialog will look like Figure 31 showing 100% completion.

FIGURE 31. Simuation Tool after Starting

	Simulator Tool
	Simulation mode: Functional 🗨 Generate Functional Simulation Netlist
	Simulation input: E:/Tutorials/MyFin_roject/myfirstproject.vwf
Stem	Simulation period     Simulation until all vector stimuli are used     G. End simulation at Lease
D)	Simulation options
No toro	Automatically add pins to simulation output waveforms
- ATAN	Setup and hold time violation detection
	<ul> <li>☐ Glitch detection: 1.0 ns ▼</li> <li>✓ Overwrite simulation input file with simulation results</li> </ul>
	100 %
	00:00:02
	🔭 Start 💿 Stop 🤨 Open 🕀 Report
	e on ve

21. Now bring focus to the myfirstproject.vwf window and view the results. Notice that the QOut waveform has been created according to the DFF function. Notice that there are no FPGA delays. The output is seen immeadiately on the rising edge of the ClkIn. See Figure 32.

	nyfirstproj			0.75	<b></b>	00.05
Mast	er Time Bar:	25.0 ns	● ● Pointer:	2.75 ns	Interval:	-22.25 ns
	Name	Value at 25.0 ns	0 ps		10.	Ons
	ClkIn	B 0				
	Dln	B 0				
$\odot$	QOut	B 1				
22		with the r	least of the tool	horioona	to Zoom	In/Out and
22		the inputs.	est of the tool	bar icons		i in/Out and
23	. To simul	-	simply click or Tool.	n the <b>Star</b>	t Simula	t <b>ion</b> icon or
24	. Now in t	the <b>Simula</b>	ation Tool ch	ange the	simulatio	on mode to

#### FIGURE 32. Simulated Waveform Output

24. Now in the **Simulation Tool** change the simulation mode to Timing and click on Start. Now the myfirstproject.vwf window will show delays that are incurred. Use the tools to see that the ClkIn to QOut delay is 6.91ns.

# Section 5: Programming the FPGA

Compilation generates a number of files; but, the files to use to programming the FPGA are either the .sof or .pof files. Hence, there are two ways to program the Cyclone FPGA on the board.

- JTAG programming mode. In this mode, only the .sof may be downloaded while the system is powered. Once the system is powered down, the FPGA will lose it's programming.
- Active Serial mode. This mode produces a more permanent result using the .pof file. An Altera EPROM is programmed and upon power-up the FPGA will be programmed with the contents in the EPROM.

Before setting using the mode first the programming hardware must be configured. The step below show how.

1. Choose **Programmer** from the Tools menu. A new Chain Description file (.cdf) opens in the Programmer window automatically listing the myfirstproject.sof file as the current programming file with the mode selected as JTAG and hardware setup set to No Hardware. As shown in the Figure 33.

FIGURE 33. Programming Window

🔔 Hardware Setu	Jp No Hardware			Mod	le: JTA
Mu Start	File	Device	Checksum	Usercode	Progra
Stop	1ject/myfirstproject.sof	EP1C6Q240	000875F2	FFFFFFF	
Auto Detect					
🗙 Delete					
🍰 Add File					
Change File					
Save File					
Add Device					
1 Up					
Down					

	og box pops up as IRE 34. Hardware S			
Hardw	vare Setup			
Hardy	vare Settings JTAG Settin	ngs		
Sele	ct a programming hardware ware setup applies only to	e setup to use wi the current progr	hen programming de rammer window.	evices. This programming
Contraction of the second s	ently selected hardware: ailable hardware items:	No Hardware	0	
	Hardware	Server	Port	Select Hardware
				Add Hardware
				Remove Hardware
AGI -				Close
	92			Close
3.	Click on the Sele	ect Hardw	r <b>are</b> button.	
( )	Click on the <b>Sele</b> ialog box	ect Hardw	v <b>are</b> button.	
d	A REPORT OF A R		vare button.	
d	ialog box JRE 35. Add Hardwa		rare button.	Figure 35 shows t
d	ialog box		vare button.	Close Figure 35 shows t
d	ialog box JRE 35. Add Hardwa	are	r <b>are</b> button. MV or ByteBlaster	Figure 35 shows t
d	ialog box JRE 35. Add Hardwa	are ByteBlaster		Figure 35 shows t
d	ialog box JRE 35. Add Hardware Add Hardware Hardware type:	are		Figure 35 shows

FIGURE 36. Selected Hardware

- 4. Select the type of hardware from the drop down list and also select the port. Then click on **OK**.
- 5. Now under the Available Hardware Items, the hardware type is seen. In this example it is ByteBlaster. Click on the **Byte-Blaster** and then click on **Select Hardware**.
- 6. Now under the Currently selected hardware: ByteBlaster[LPT1] is seen as shown in Figure 36. Click on **Close**.

Select a programming hardware setup to us hardware setup applies only to the current p Currently selected hardware: ByteBlast		vices. This programmi
	Jogrammer window.	
	0.0711	
Available hardware items:	er [LPT1]	
Hardware Server	Port	Select Hardw
ByteBlaster Local	LPT1	Add Hardwar
		Remove Hard
		- Homoro Hora

The hardware is now setup and progamming can occur.

Note: Make sure the programming hardware is connected to the computer to proceed with the next steps.

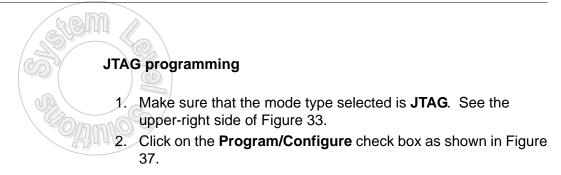


FIGURE 37. JTAG Programming

		< FAG			
🚖 Hardware Setup	ByteBlaster [LPT1]			Mod	le: JTAG
Mu Start	File	Device	Checksum	Usercode	Program/ Configure
Stop	ject/myfirstproject.sof	EP1C6Q240	000875F2	FFFFFFF	<b>V</b>
Auto Detect					
X Delete	Step 4				
灅 Add File				Step 2	
👺 Change File					
Save File					

- 3. Connect the Byte Blaster Cable to JTAG connector header (JP12) on the board.
- 4. Click Start as shown in Figure 37 to program the FPGA.

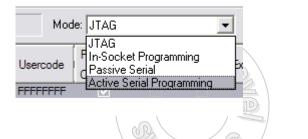
As soon as the programming starts, percentage will get displayed in the Progress bar. After it reaches 100%, the Config done LED will glow on the board.

The FPGA is now programmed and now using the Push Button and DIP Switch, the DFF functionality may be implemented to turn on and off the LED. Skip to Section 6.



1. Select Mode as **Active Serial Programming** as shown in Figure 38.

FIGURE 38. Select Active Serial Programming



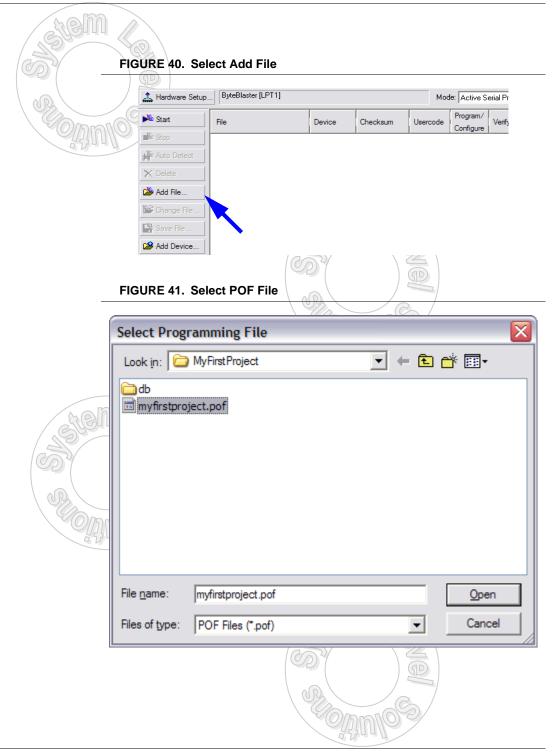
2. When switching over from JTAG to ASP, a dialog box like one shown in Figure 39 ask to clear all devices. Click **Yes**.

### FIGURE 39. Change Dialog

urrent device list cannot be added to selected programming mode Active Serial Programming. all devices in current device list and switch to selected mode?
<u>No</u>

4. Now the Select Programming File dialog box appears so select **myfirstproject.pof** and click **Open**. Now the .pof file is added to the file list. Figure 41 shows the details.





- 8. Click on the **Program/Configure** check box as shown in Figure 37.
- 9. Connect the Byte Blaster Cable to Active Serial header (JP11) on the board.
- 10. Click Start as shown in Figure 37 to program the FPGA.

Note: While downloading .pof file, if some error occurs then check that the selected configuration device is EPCS1. In order to do this, select Settings under Assignments menu, Click on Device & Pin Options. Under General option select Generate Compressed bitstreams option. Then select Configuration option. Under that select the Configuration Scheme as Active Serial. Select the Configuration Device as EPCS1. See section 3 Figure 16 and 17 as well as the associated text.

Now the EPCS1 EPROM has been programmed so each time the board is powered the myfirstproject design will be loaded into the





## Section 6: Using the Hardware

Testing the design is very easy to perform as all the components are found on the lower left corner of the board. Make sure the board has been programmed with either mode.

Note: When the board is first programmed, the D3 LED does not glow. Since the LEDs are active high, they glow only when a "1" is provided. Also note that on the DIP Switch the "On" position provides a "0" to the FPGA. See the board reference manual for more information.

- 1. Find Push Button SW4
- 2. Find DIP Switch SW3 Postion 1
- 3. Find LED D3
- 4. Toggle DIP Switch SW3 Postion to the OFF position if not already there.
- 5. Press Push Button SW4
- 6. The LED D3 will turn On.
- 7. Toggle the DIP Switch and press the Push Botton to turn On and Off the LED.

Remember the Push Button generates an edge for the DFF as it is connected to ClkIn and the DIP Switch is the DIn.

