Designing a NiosII System from Scratch for UP3

Tutorial

Version 01.00

System Level Solutions Inc. (USA)

14702 White Cloud Ct.
Morgan Hill, CA 95037

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About this manual

This tutorial provides all the steps for creating a Nios II processor system from the scratch for UP3. Also it shows how to create, compile, debug and run a C/C++ program using the Nios II IDE.

How to find the information

- The Adobe Acrobat Find feature allows you to search the contents of a PDF file. Use Ctrl + F to open the Find dialog box. Use Ctrl + N to open to the Go To Page dialog box.
- Thumbnail icons, which provide miniature preview of each page, provide a link to the pages.
- Links allow you to jump to related information.

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TABLE 1. Contact Information

Information Type	E-mail
Product literature services, SLS literature services, Non-technical customer services, Technical support.	support@slscorp.com

Introduction

This tutorial walks you through the hardware & software development flow. It shows you how to use SOPC Builder and the Quartus II software to create and use your own Nios II system

This tutorial is basically for users who are new to the Nios II processor as well as users who are new to the concept of using embedded systems in FPGA's. This tutorial guides you through the steps necessary to create and compile a 32-bit Nios II system design, called nios2_in_up3. This simple, single-master Nios II system consists of a Nios II embedded processor and associated system peripherals as well as interconnections for use with the input & output hardware available on the UP3 board.

This tutorial is divided into the following three sections:

- 'Designing & Compiling' - Teaches you how to use SOPC builder to create the Nios II system module in block design file (.bdf) and how to compile the Nios II design using the Quartus II Compiler.
- 'Programming' - Teaches you how to use the Quartus II Programmer and the USB-Blaster cable to configure the FPGA on UP3 board. It also teaches you how to store the design in PROM (EPCS1) provided on the board, so that the FPGA can be configured with your design whenever power is applied to the board.
- 'Running the Software on Your Nios II System' - Provides the instructions for running software on your Nios II system using the Nios II integrated development environment (IDE).

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Hardware & Software Requirements

The user will require following hardware & software

- A PC running with Win 2000/XP OS
- Nios II embedded processor
- The Quartus II software version 4.0 SP1 or higher
- UP3 Education Kit or Nios Development boards.
- Altera USB Blaster/Byte Blaster download cable

Designing and Compiling

To use the instructions in this section, you need to be familiar with the Quartus II software interface-specifically toolbars. Refer to Quartus II help for more information about using the Quartus II software.

Creating a Quartus II Project

Here are the steps to create a new Quartus II project:

1. Open the Quartus II.
2. Choose File>New Project Wizard..
3. Click Next.
4. Select Working Directory of the Project, Name of the project as ‘nios2_in_up3’ & top-level entity as ‘nios2_in_up3’. Then Click Next.
5. Click Next.
6. Click Next.
7. Select the family as ‘Cyclone’ and highlight the Yes combo box. Click Next.
8. We will select the FPGA for UP3 board (which is Cyclone EP1C6Q240C8), so under Filters / Speed Grade select 8. Then under Available devices: highlight ‘EP1C6Q240C8’. Click Next.
9. Click Finish.

Start SOPC builder

SOPC builder is a software tool that allows you to create a fully functioning, custom-embedded micro controller called the Nios II system module. A complete Nios II system module contains a Nios II embedded processor and its associated peripherals.

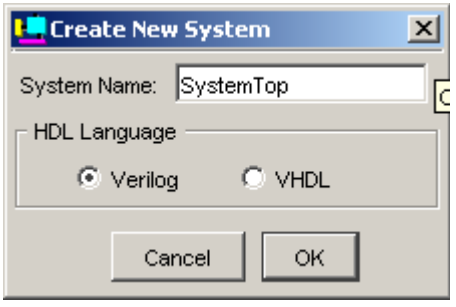
To start SOPC builder, perform the following steps:

1. Open the Quartus II software.

2. Choose SOPC Builder (Tools menu). SOPC Builder displays the Create New System dialog box.
3. Type ‘SystemTop’. See Figure 1
4. Specify Verilog or VHDL in HDL Language field.

SOPC Builder generates plain text Verilog HDL or VHDL for all of its native components depending on the language you choose.

FIGURE 1. Create New System dialog box

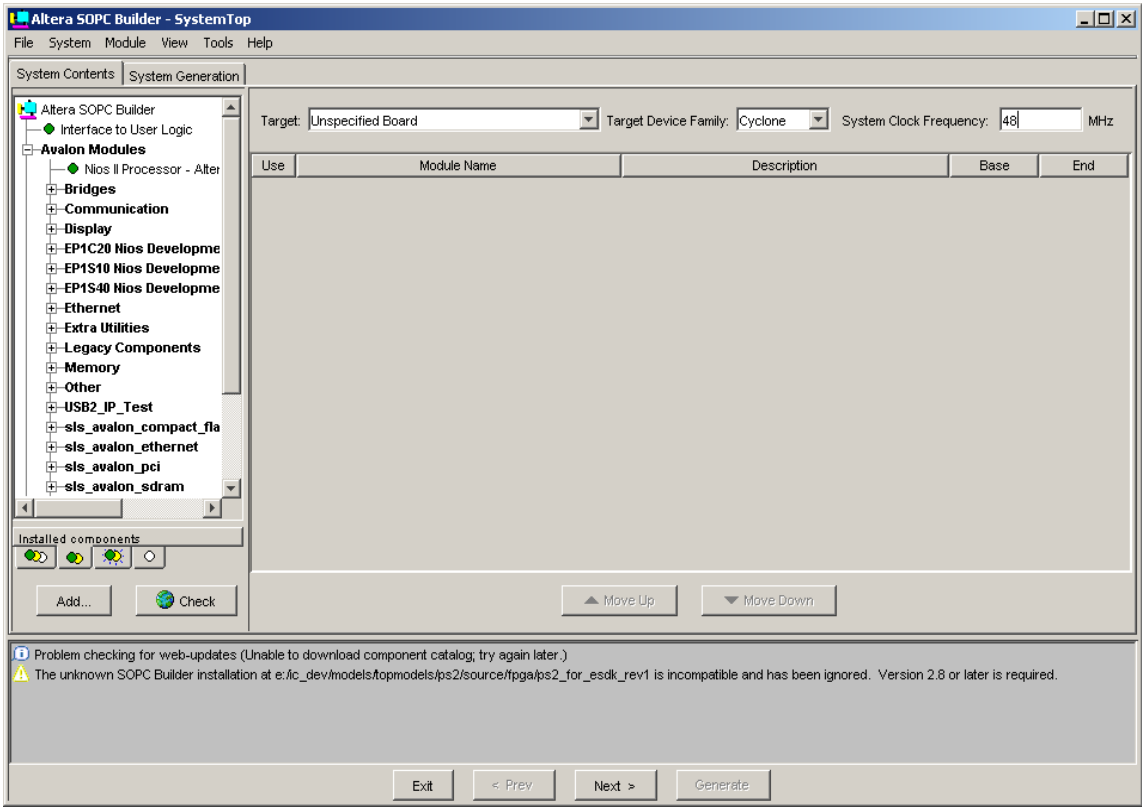


5. Click OK. The Altera SOPC Builder - SystemTop window appears and the System Contents tab is displayed.

You are now ready to set the speed and add the Nios II CPU and peripherals to your system. The components you will be adding are located in the module pool on the left hand side of the System Content tab. See Figure 2.

The functionality of the SOPC Builder system depends on the hardware on which it will run. Thus, specifying the target board is the first step in creating a system

FIGURE 2. SOPC Builder



Specify Target Hardware Settings

The functionality of the SOPC Builder system depends on the hardware on which it will run. Thus, specifying the target board is the first step in creating a system.

- Choose a board type in the Target pull-down menu, As UP3 is not yet added in the menu, keep the ‘Unspecified Board’.
- Select the System Clock Frequency as 48Mhz.

Adding CPU & Peripherals

This section describes adding following modules to the SOPC Builder.

- Nios II 32-bit CPU
- JTAG UART
- Timer
- Avalon Tri State Bridge
- SLS_UP3_SRAM
- LED_PIO

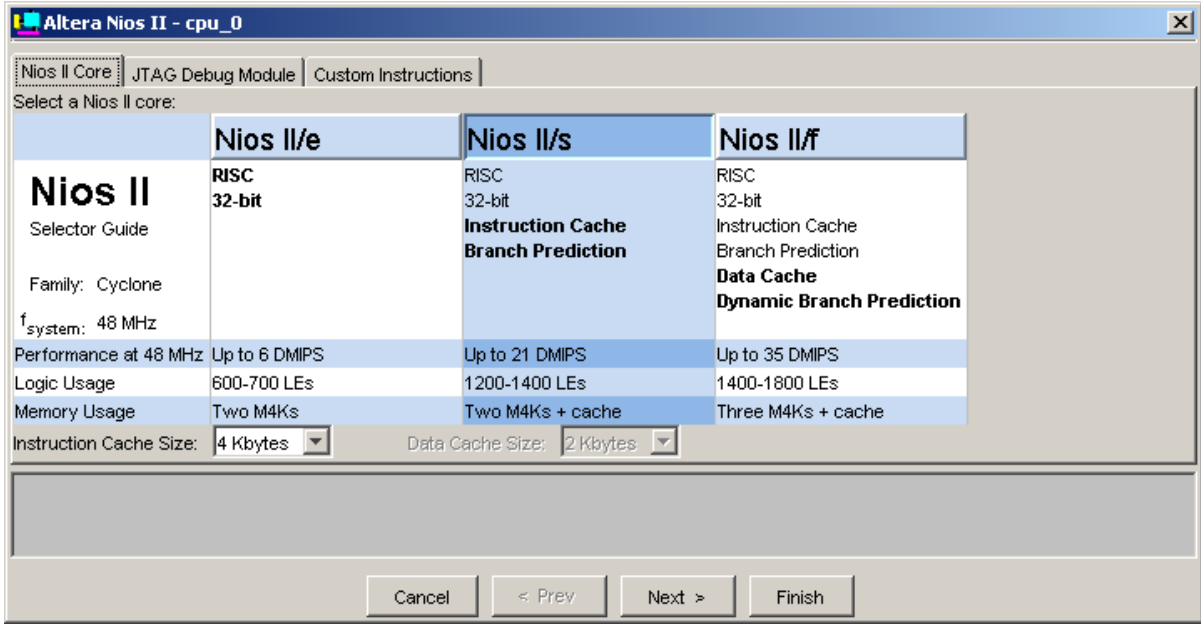
Nios II 32-bit CPU

To add the Nios II 32-bit CPU, named CPU, perform the following steps:

1. Under Avalon Modules, select Nios II Processor - Altera Corporation.
2. Click Add. The Nios II configuration wizard titled Altera Nios II - cpu_0 displays.
3. Specify the following options in the Nios II Core tab.

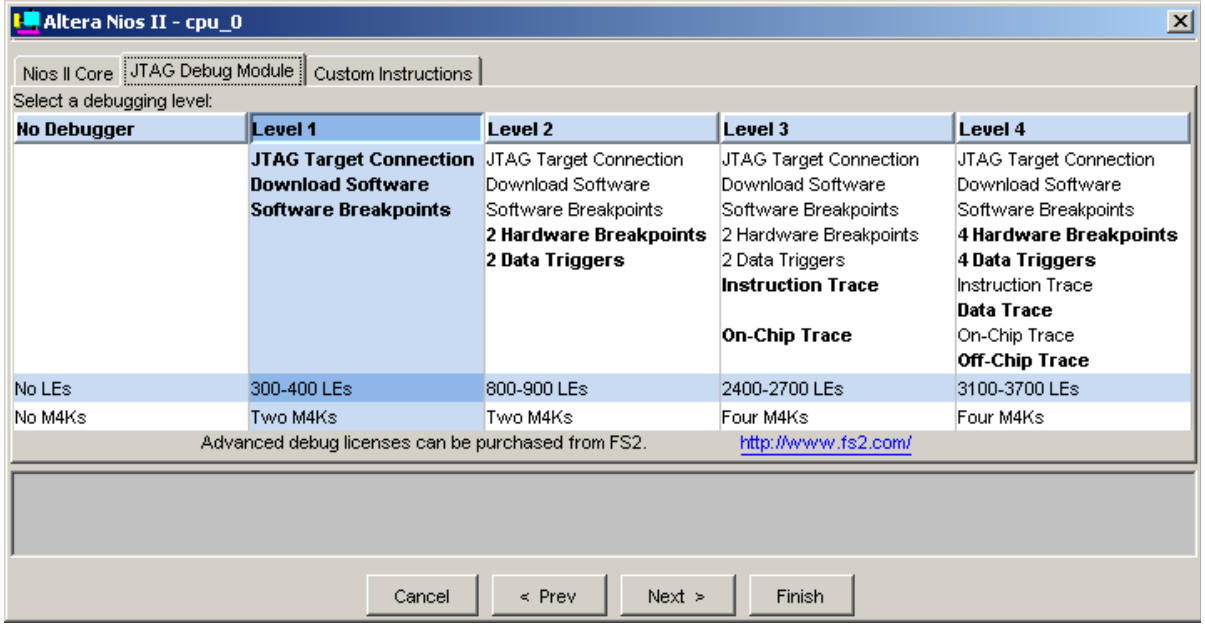
- Select the processor core: Nios II/s as in Figure 3
- Instruction Cash Size: 4Kbytes

FIGURE 3. Nios II



4. Click the JTAG Debug Module tab and choose the highlighted tab shown in Figure 4.

FIGURE 4. Nios II Options



5. Click Finish and returning you to the main SOPC Builder window.

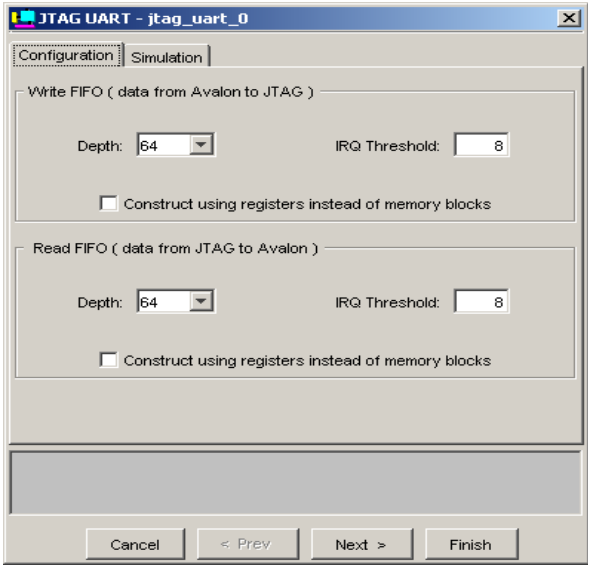
You will see errors in the SOPC Builder message display. However, the issue causing the errors are resolved when the rest of the elements are added to the design. At this stage error messages can be safely ignored.

JTAG UART

The JTAG UART interface component is added to reduce the number of connections necessary to 'talk' to the NIOS II. To add it

1. Select Communication > JTAG UART and click Add.. The JTAG UART - jtag_uart_0 wizard displays as shown in Figure 5.

FIGURE 5. JTAG UART



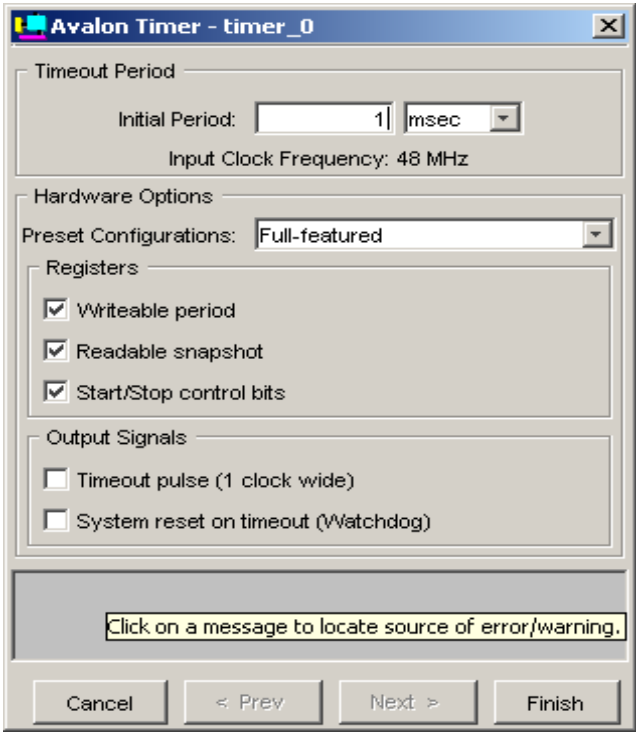
2. Accept the default options by clicking Finish.

Timer

The Timer is necessary for some of the default device drivers provided in the HAL system library. For example, the JTAG_UART. To add the timer perform the following steps:

1. Choose Other > Interval Timer and click Add.
2. Leave the default settings in the Avalon Timer - timer_0 window. Figure 6.

FIGURE 6. Timer



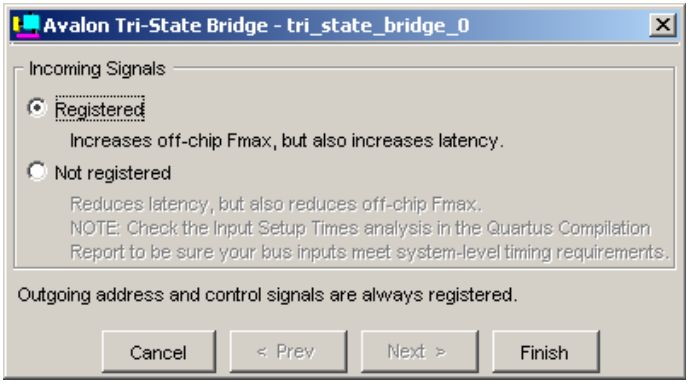
3. Click Finish.

External RAM Bus (Avalon Tri-State Bridge)

For the Nios II system to communicate with memory external to the FPGA on the Nios development board, you must add a bridge between the Avalon bus. To add this:

1. Select Bridges > Avalon Tri-State Bridge and click Add. The Avalon Tri-State Bridge - tri_state_bridge_0 wizard displays. See Figure 7.

FIGURE 7. Avalon Tri-State Bridge



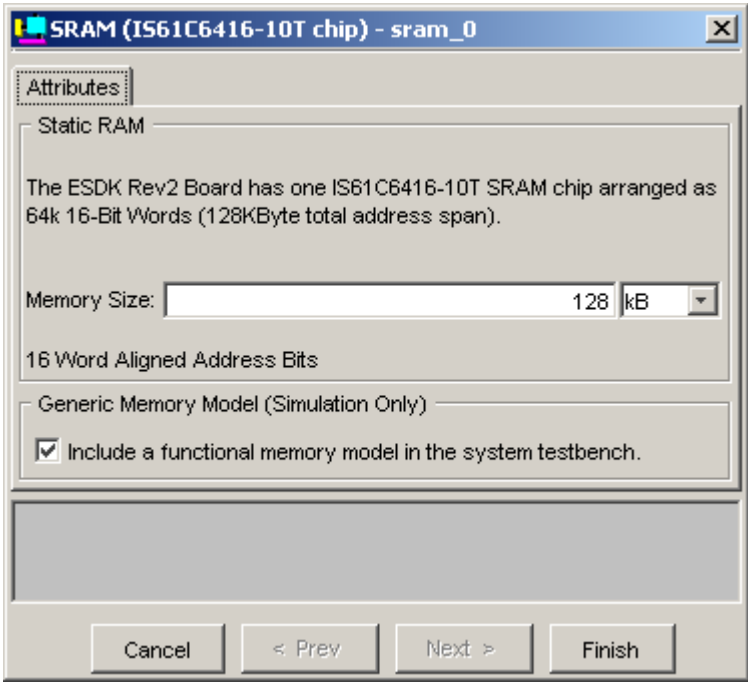
2. Click Finish.

SLS_UP3_SRAM

Depending on which hardware you are using user has to select the external SRAM or any memory. To add SLS_UP3_SRAM perform the following steps:

1. Select Memory > SLS_UP3_SRAM and click Add.
2. The SRAM (IS61C6416-10T(OR equivalent) chip) - sram_0 wizard displays. See figure 8.

FIGURE 8. UP3 SRAM



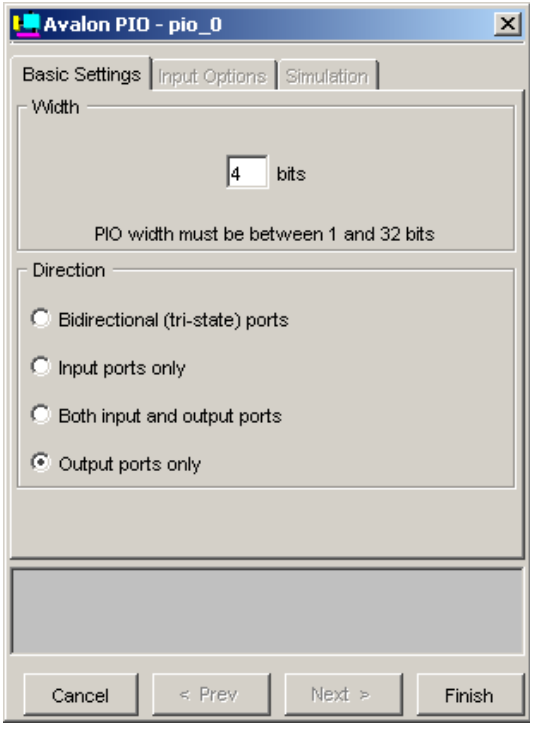
3. Click Finish.

LED PIO

To provide an interface for LED's on UP3 Kit, add the LED PIO by performing the following steps:

1. Select Other > PIO (Parallel IO) and click Add.
2. Specify the Options: Width = 4 and Direction = Output port only. See Figure 9.

FIGURE 9. LED PIO



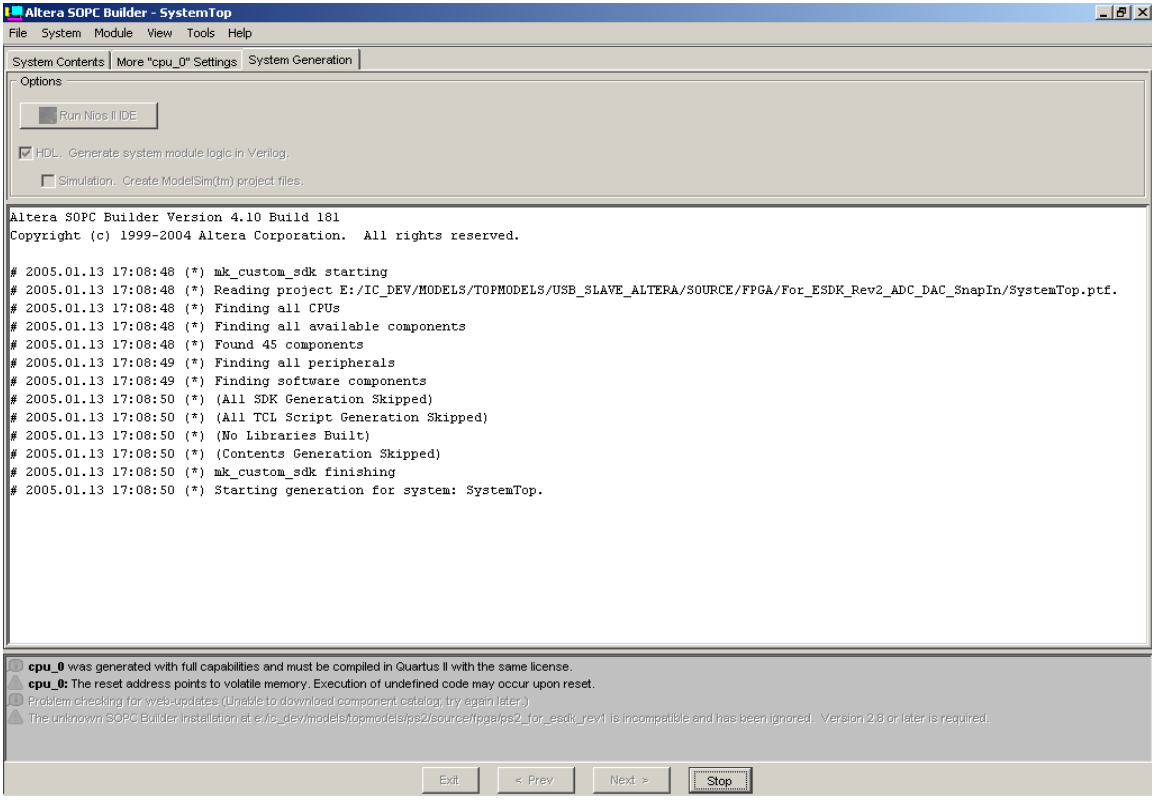
Generating the System

To generate the design logic, perform the following steps.

1. Click the System Generation tab.
2. Specify the following settings from the Options window. Figure 10

- HDL: Check this box
- Simulation: Check this box if you have Modelism installed and would like to simulate the design.

FIGURE 10. Generating the System



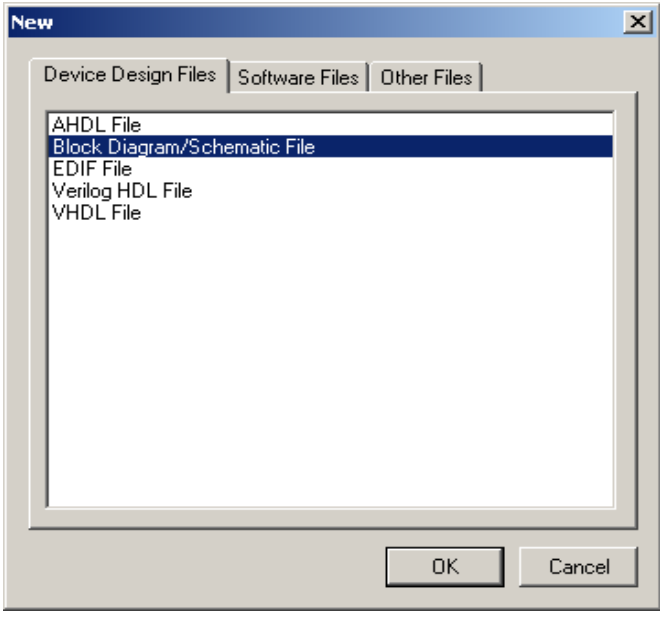
3. Click Generate. See Figure 10.
4. When generation is complete, the SYSTEM GENERATION COMPLETED message displays. DO NOT EXIT SOPC BUILDER AT THIS POINT. We will return to this window prior to testing the system with software.

Adding the Quartus II Symbol to the BDF

During generation, SOPC Builder creates a symbol of the System-Top, for use in Quartus II. To add the symbol perform the following steps:

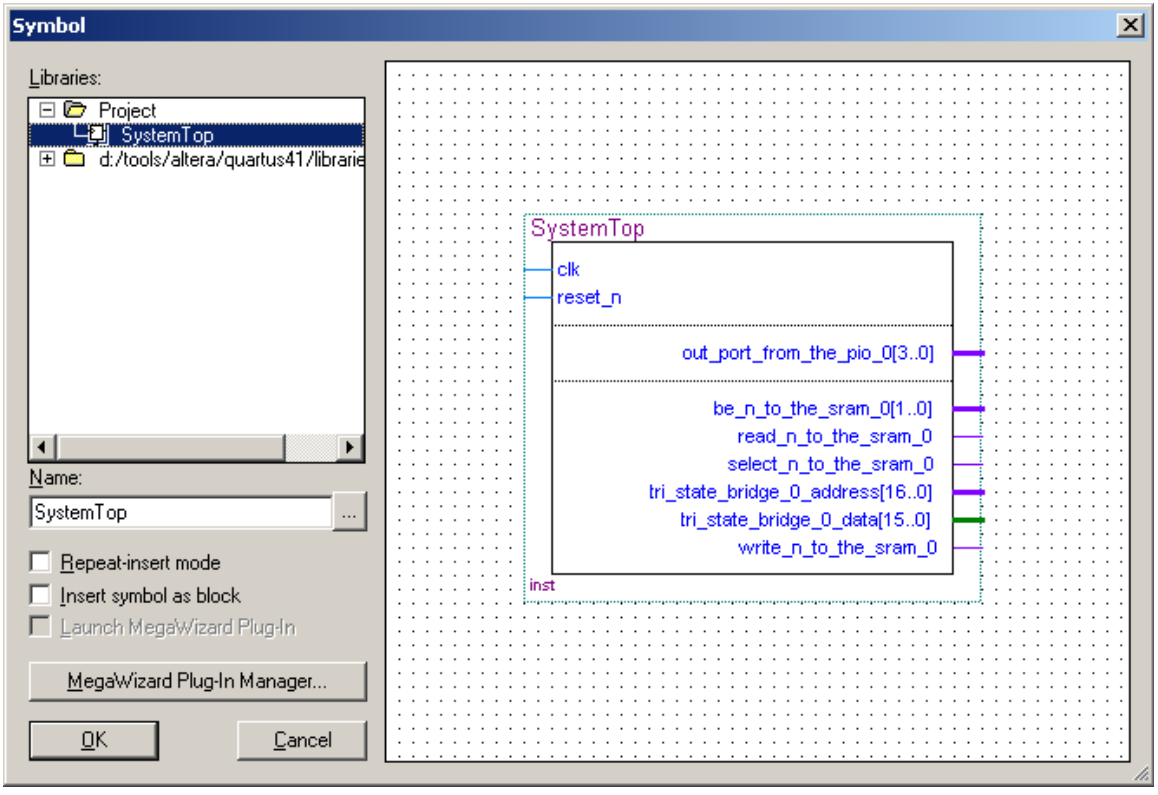
1. Select File (menu) > New.
2. Under Device Design Files, highlight Block Diagram/Schematic File. See Figure 11.

FIGURE 11. New Block Design File



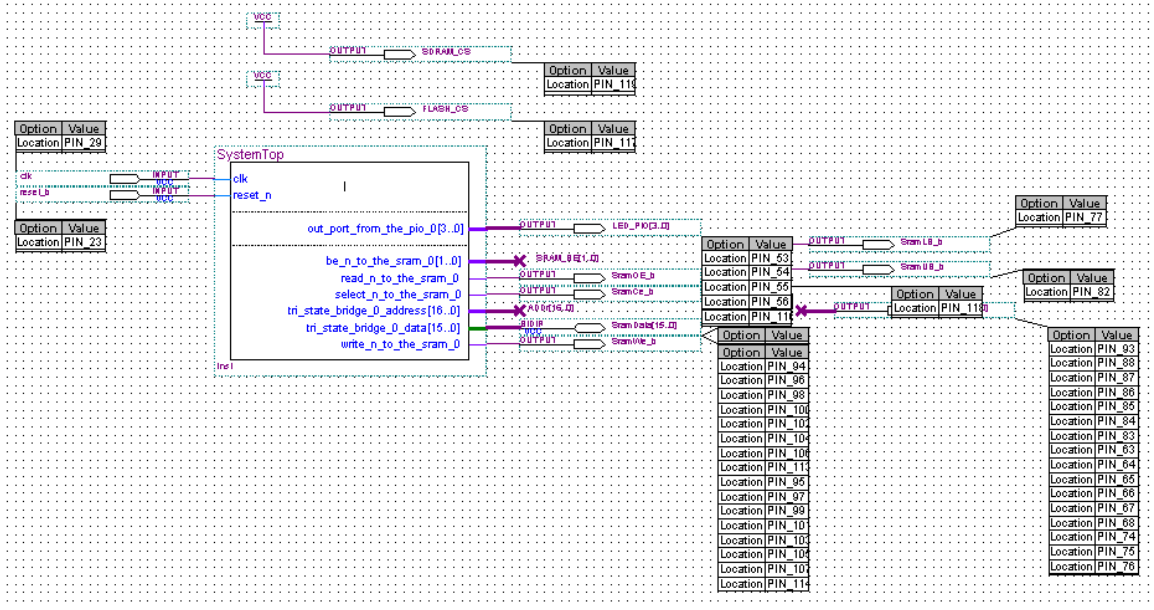
3. Click OK.
4. Return to the Quartus II software and double click anywhere inside the BDF window. The Symbol dialog box appears. See Figure 12.

FIGURE 12. BDF Dialog box



5. From Libraries, expand the Project directory by clicking the + sign next. See Figure 12.
6. Click SystemTop. A large symbol will appear representing the Nios II system module you just created. See Figure 12.
7. Click OK. The Symbol dialog box closes and an outline of the SystemTop symbol is attached to the pointer. See Figure 12.
8. Place the symbol so it lines up with the pins that are already in the block design schematic files.
9. Choose Save.
10. After adding Inputs/Outpus, Inouts and pin assignments the final BDF looks like Figure 13. Please refer the provided Reference Design.

FIGURE 13. Final BDF



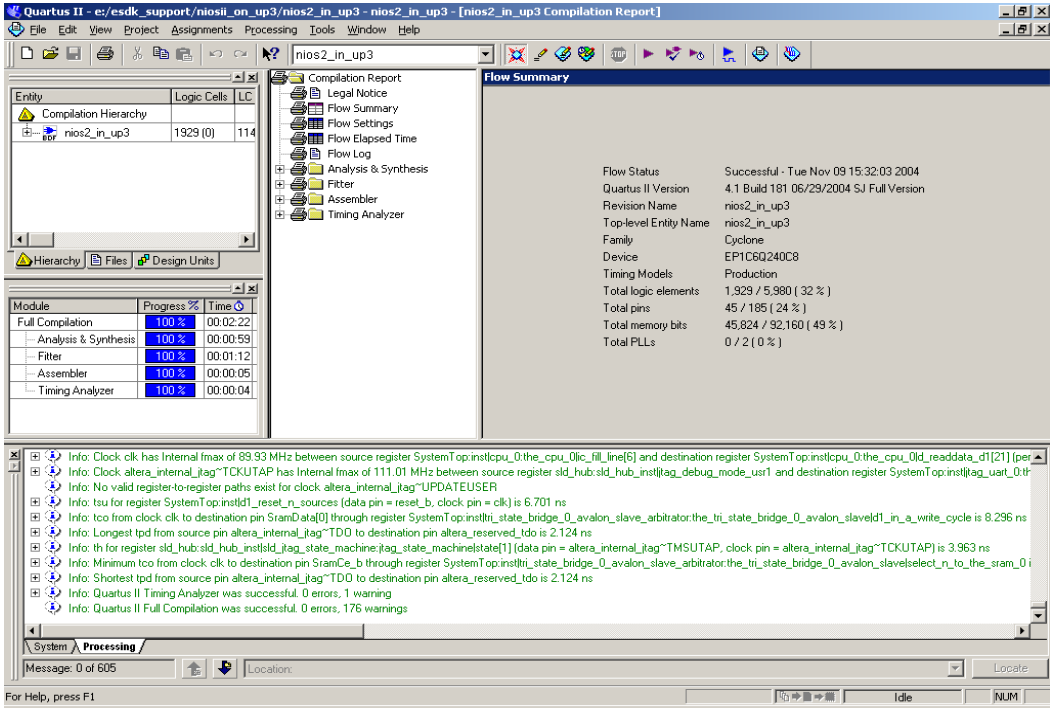
Compiling the Design

During compilation, the Compiler locates and processes all design, project files, generates messages and reports related to the current compilation, creates the SRAM object file (.sof) as well as any optional programming files.

To compile the nios2_in_up3 design, follow these steps:

1. Choose Start Compilation (Processing menu), or click the Start Compilation toolbar button. If you get a message asking if you want to save the changes you made the BDF file, choose Yes.
2. When compilation completes, you can view the results in the nios2_in_up3 Compilation Report window. See Figure 14.

FIGURE 14. Compilation Report Window



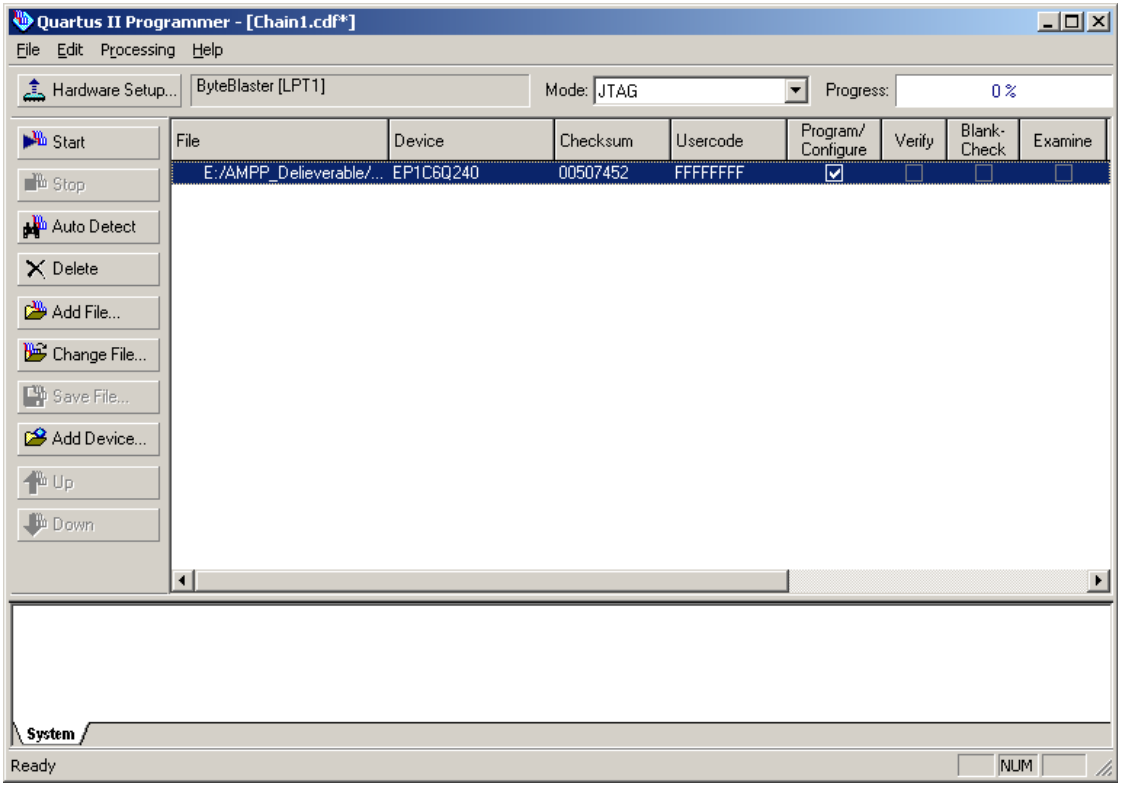
Programming

After successful compilation, the Quartus II Compiler generates one or more programming files that the Programmer uses to program or configure a device.

To program your design, perform the following steps.

1. Choose Programmer (Tool menu). The Programmer window opens.
2. In the Mode list of the programmer window, make sure JTAG is selected.
3. Click Hardware Setup.. to configure the programming hardware. The Hardware Setup dialog box appears.
4. From the Hardware column, select USB Blaster or Byte Blaster, which you are using.
5. Click Close to exit the Hardware Setup window.
6. In the Programmer window, turn on Program/Configure. See Figure 15.
7. Click Start.

FIGURE 15. Programmer Window



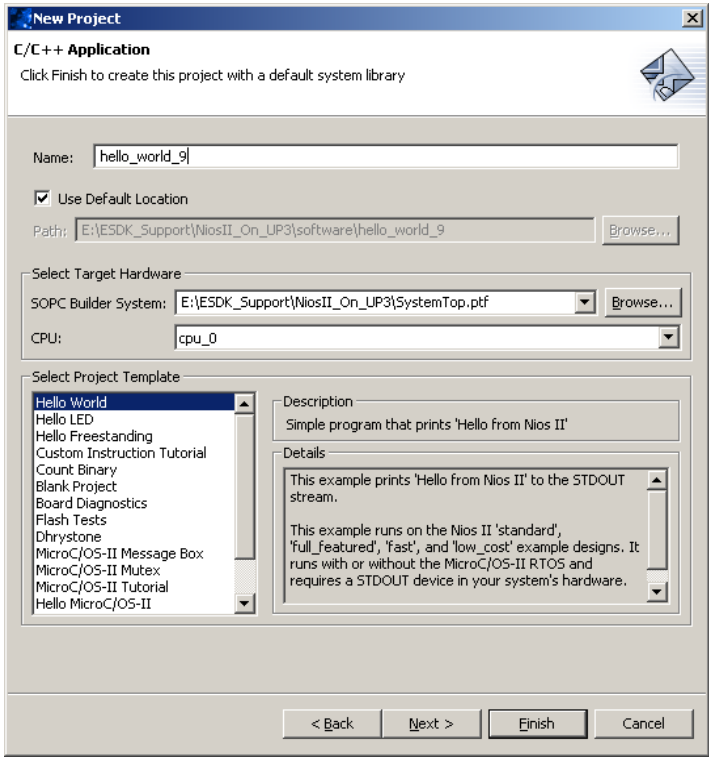
Running NiosII IDE

We will be using Nios II Integrated Development Environment (IDE) to run our software on top of Nios II System. To start the Nios II IDE from the Quartus II software, perform the following steps:

Creating the Software

1. Click the System Generation tab of the SOPC Builder, then click the Run Nios II IDE button.
2. From the opening window, choose File > New C/C++ Application.
3. Highlight Altera Nios II & C/C++ Application & Click Nextt.
4. Keep the setting as shown in Figure 16.

FIGURE 16. New Project



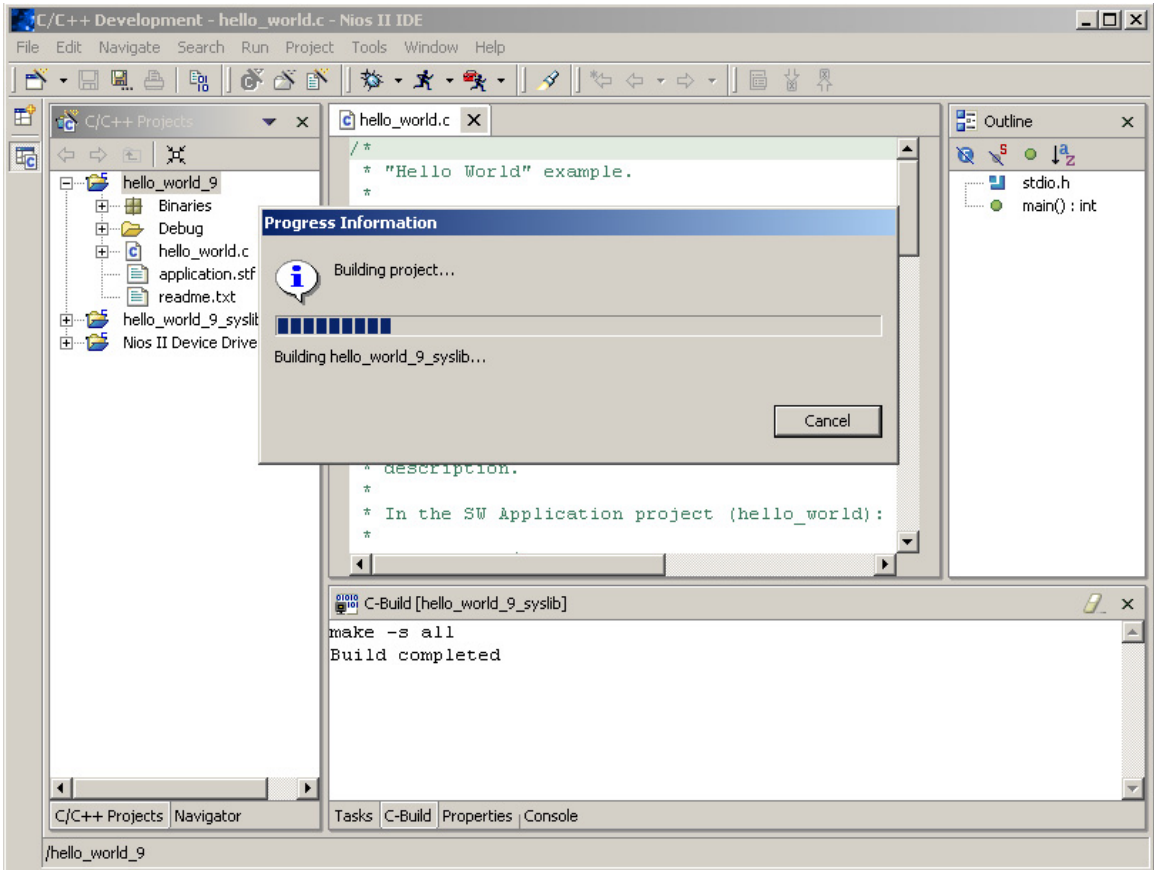
5. Click Finish.

Building the Software

Perform the following steps:

1. To build your project, right click on your project in the navigator pane and select Build Project. See Figure 17.
2. When the build process successfully completes, you can run the project.
3. See Figure 17.

FIGURE 17. Building the project



Running the Program

To run your program on the development board, perform the following steps:

1. Choose Run > Run.. in the main Nios II IDE window.
2. Double Click on Nios Ii Hardware in the Configurations browser on the left-hand side. The run window displays.
3. If you have more than one JTAG cable connection, then you will need to select the Target Connection tab and choose the cable that is connected to your board from the JTAG cable pull down menu.
4. Accept the default and click Run.

FIGURE 18. Running the program

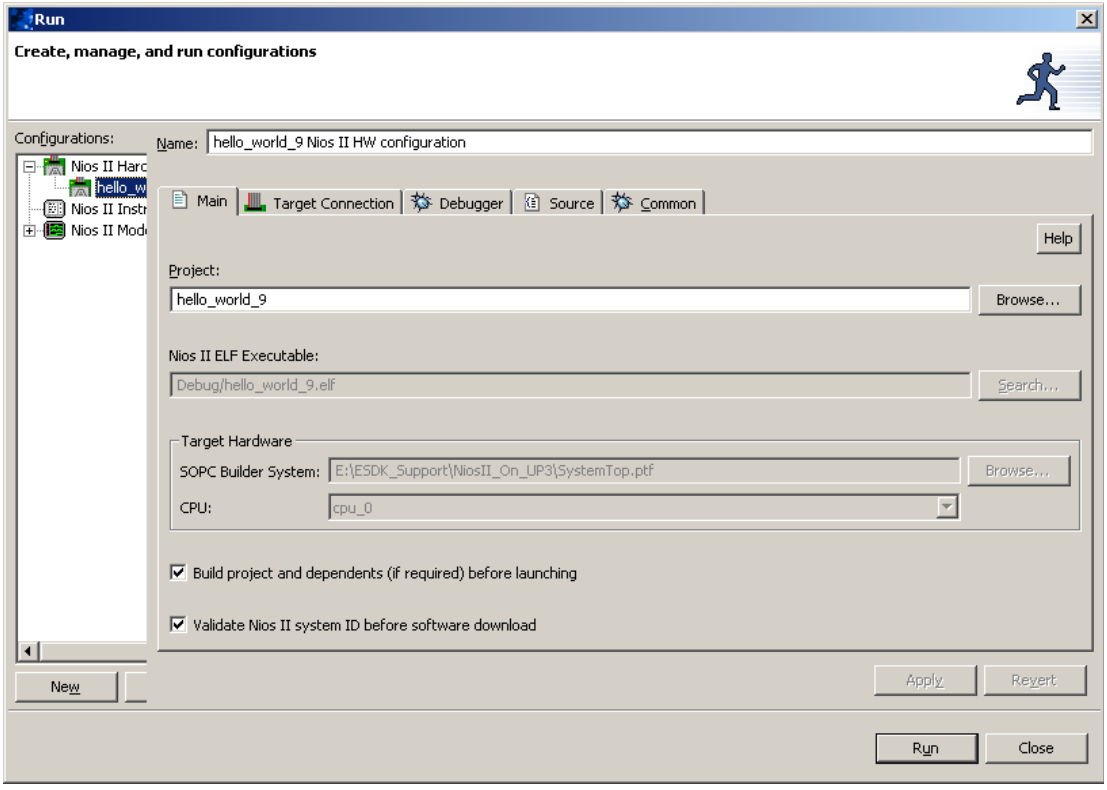
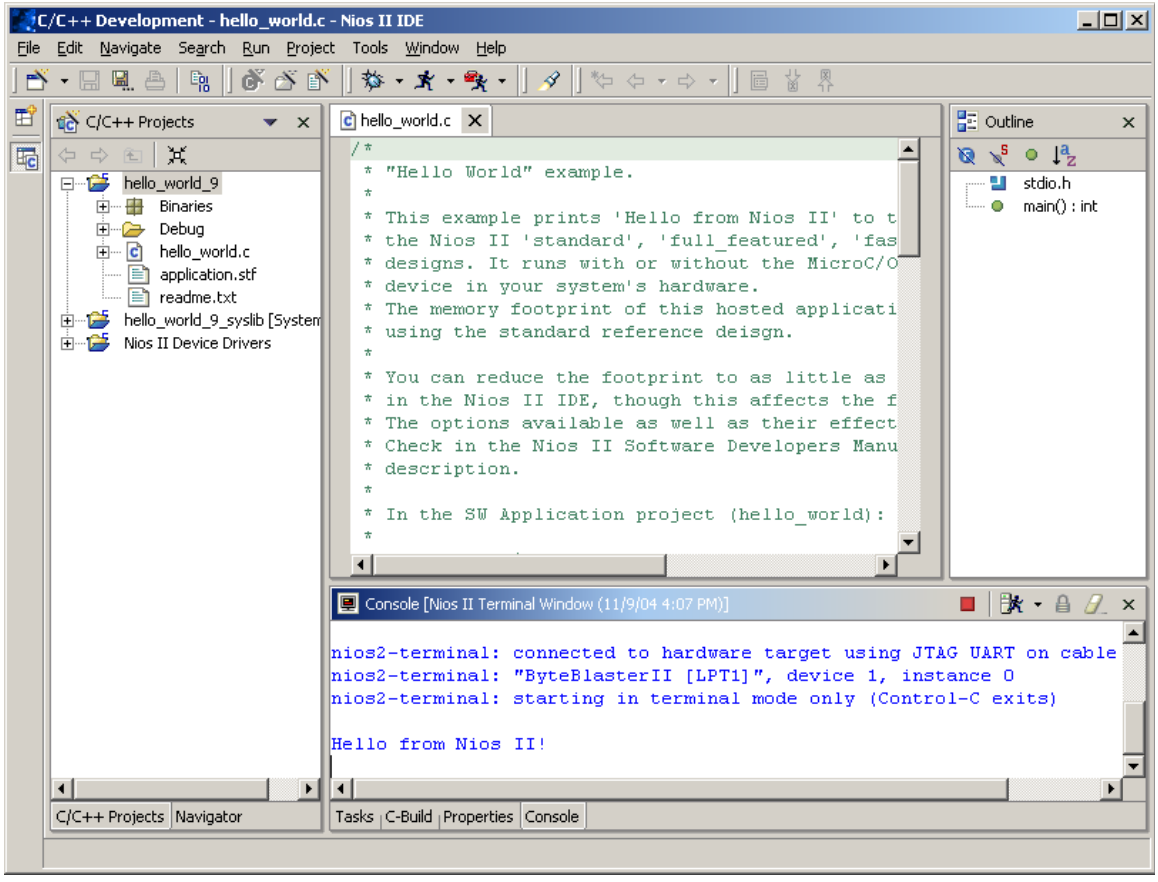


FIGURE 19. Hello world on hardware



On Clicking **Run,** the Nios II IDE downloads the software, resets the processor, and starts execution of the software. At some point, the Nios II IDE “running” window displays with a message in the console window. See Figure 19.

For the above case, user will see “Hello from Nios II!” in the console window. Provided there are no errors during Compilation and the run process.

Now try using the NIOS II IDE to glow the LEDs on the UP3 board. HINT: Look at the memory map created by the SOPC builder.