Score:	Name:

ECE 3055 Quiz 9 - Wednesday, November 3

In the space below, draw a block diagram of the hardware synthesized by the VHDL code found on the additional page provided with the quiz. In the block diagram, include the following:

- 1. Show all input signals on the left and outputs on the right.
- 2. Draw each hardware unit in a style similar to the textbook's block diagrams.
- 3. Include and clearly indicate any registers, clock signals, and resets.
- 4. Label all signals with their VHDL signal name (both internal and external).
- 5. Use a "/" with a number to indicate the width of any busses (more than 1-bit).
- 6. Number each of the mux's input signals with it's corresponding decimal number (i.e. the value on the mux's control input signal that selects each input).
- 7. Indicate # of bits and direction for any shifts and indicate if resets are sync or async.

Inputs Hardware Outputs

