Score:	Name:		

## ECE 3055 A Quiz 1 - Spring 2005

The following RISC assembly language program is executed on a MIPS processor. Fill in the register values that will be present, after execution of this program. A summary of MIPS instructions is included at the bottom of the page – for anyone unfamiliar with the MIPS instruction set. Prior to execution of the program, memory location 0x01000 contains 0x30552031. Note: 0x indicates hexadecimal and all answers must be in hexadecimal, default is decimal in the MIPS assembly language source file. A MIPS memory word or register contains 32-bits. Use XXXXXXXXX for an undefined value.

	LW	\$3, 0x01000
	SLL	\$4, \$3, 4
	AND	\$3, \$4, \$3
	ADD	\$2, \$3, \$4
	LUI	\$5, 0x3055
	ORI	\$5, \$5, 37
	SUB	\$6, \$4, \$3
	BNE	\$3, \$6, LABEL1
	ADDI	\$6, \$0, -2
LABELI:	$\mathbf{s}\mathbf{w}$	S6, 0x01000

After execution of the MIPS code sequence above,

$$R2 = 0x G5 A 2 O3 2 O$$
 (in hexadecimal)

$$R3 = 0x$$
  $0050000$  (in hexadecimal)

$$R4 = 0x^{6} 5520313$$
 (in hexadecimal)

$$R5 = 0x$$
 30550025 (in hexadecimal)

2 pts. each

Memory Location 0x01000 contains: 0x 05020300 (in hexadecimal)

The MIPS processor contains thirty-two 32-bit registers, \$0 through \$31. So always contains a zero. By default, all arithmetic operations use two's complement arithmetic. Assume no branch delay slot is present.

MIPS Instruction			Meaning
ADD	Rd, Rs, Rt	-	Rd = Rs + Rt (R - register(S))
AND	Rd, Rs, Rt	-	Rd = Rs bitwise logical AND Rt (R - register (S))
ORI	Rd, Rs, Immed	•	Rd - Rs bitwise logical OR Immediate waltue
LUI	Rd, Immed	-	Rd - 16-bit Immediate value high 16-bits, 0's low 16-bits
BNE	Rs, Rt, address	-	Branch to address, only if Rs not equal to Rt
LW	Rd, address	-	LOAD - Rd gets contents of memory at address
SRL.	Rd, Rs, count	-	Shift right logical (use 0 fill) by count bits
SUB	Rd, Rs, Rt	-	Rd = Rs - Rt
SW	Rd, address	-	STORE - memory at address gets contents of Rd
XOR	Rd, Rs, Rt	-	Rd = Rs bitwise logical XOR Rt