Score:	Name:	
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ECE 3055 A Quiz 1 - Fall 2002

The following RISC assembly language program is executed on a MIPS processor. Fill in the register values that will be present, after execution of this program. A summary of MIPS instructions is included at the bottom of the page – for anyone unfamiliar with the MIPS instruction set. Prior to execution of the program, memory location 0x0400 contains 0x20303055. Note: 0x indicates hexadecimal and all answers must be in hexadecimal. A MIPS memory word or register contains 32-bits.

2 pts / blank

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LW	\$3,0x0400
SLL	\$4, \$3, 4
ADD	\$2, \$3, \$4
AND	\$3, \$4, \$3
LUI	\$5, 0x3055
ORI	\$5, \$5, 7
SUB	\$6, \$4, \$3
BEQ	\$3, \$6, LABEL1
ADDI	\$6, \$0, -2
SW	\$6,0x0400

After execution of the MIPS code sequence above,

LABEL1:

$$R2 = 0x 23333545$$
 (in hexadecimal)

$$R3 = 0x$$
 000005 0 (in hexadecimal)

$$R4 = 0x 03030550$$
 (in hexadecimal)

$$R5 = 0x$$
 $\frac{30550007}{(in hexadecimal)}$

Memory Location 0x0400 contains: 0x FFFFFFF (in hexadecimal)

The MIPS processor contains thirty-two 32-bit registers, \$0 through \$31. \$0 always contains a zero. By default, all arithmetic operations use two's complement arithmetic.

MIPS Instruction			Meaning
ADD	Rd, Rs, Rt	-	Rd = Rs + Rt (R - register (\$))
AND	Rd, Rs, Rt	-	Rd = Rs bitwise logical AND Rt (R – register (\$))
ORI	Rd, Rs, Immed	-	Rd = Rs bitwise logical OR <i>Immediate</i> value
LUI	Rd, Immed	-	Rd = <i>Immediate</i> value high 16-bits, 0's low 16-bits
BEQ	Rs, Rt, address	-	Branch to address, only if Rs equal to Rt
LW	Rd, address	-	LOAD - Rd gets contents of memory at address
SLL	Rd, Rs, count	_	Shift left logical (use 0 fill) by count bits
SUB	Rd, Rs, Rt	-	Rd = Rs - Rt
SW	Rd, address	-	STORE - memory at address gets contents of Rd
XOR	Rd, Rs, Rt	-	Rd = Rs bitwise logical XOR Rt