**Score:\_\_\_\_\_\_ Section:\_\_\_\_\_\_\_\_\_\_\_\_ Name:\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_**

# ECE 3055 Quiz 6

1. (*1pt*) A \_\_\_\_\_\_\_\_\_*superscalar*\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_\_ processor can achieve a CPI lower than 1.
2. (*1pt*) What is the ARM Thumb instruction set and why is it used?

*A 16-bit instruction set for a 32-bit processor. It runs faster using low cost 16-bit memory in small devices.*

1. (2pts)Why does the simplest branch prediction state machine that makes sense have at least four states? *(Justify your answer)*

*Without four states it will mispredict a branch at the end of each loop incorrectly twice*.

1. (*2pts*) Explain exactly what the commit unit does in a dynamic multiple issue processor.

*The commit unit holds the results of instructions until they can be saved in order or until speculated instructions are resolved can be safely saved.*

1. (*1pt*) If the maximum speedup of a pipeline is the number of stages, why don’t you just keep adding more *stages to make it faster? (Justify your answer)*

*The longer the pipeline,the more FF setup and hold delays and uneven delays in stages become a factort.In processors, more stages increase the occurrence of data hazards, and branch hazards that force pipeline stalls.*

1. (*3pts*) Schedule/rewrite the MIPS code below minimizing stalls on the static two-issue VLIW MIPS pipeline in the textbook (page 396). Assume data forwarding and *lw* hazards work as in the final MIPS improved pipeline (i.e. Figure 4.65), but that forwarding has been added to data memory so that *sw* can immediately follow *lw* without a stall when the same register is used. Do not include loop unrolling in your solution.

**loop: LW $1,40($6)**

 **ADD $5,$5,$1**

 **SW $1,20($5)**

 **ADDI $6,$6,4**

 **ADDI $5,$5,-4**

 **BEQ $5,$0, loop**

|  |  |  |  |
| --- | --- | --- | --- |
| **Label** | **ALU/Branch** | **LW/SW** | **Clock**  |
| Loop: | ADDI $6,$6,4 | LW $1,40($6) | 1 |
|  | ADDI $5,$5,-4 |  | 2 |
|  | ADD $5,$5,$1 |  | 3 |
|  | BEQ $5,$0, Loop |  SW $1,24($5) | 4 |
|  |  |  | 5 |
|  |  |  | 6 |